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Intel Sky Lake Platform

SLK-S CPU / SLK PCH-H

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Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

PCA P/N, Scorpion/Spitfire/Toledo	
SCH P/N, Scorpion/Spitfire/Toledo	
PCB P/N, Scorpion/Spitfire/Toledo	

	
INDEX	
DWG NO	Rev
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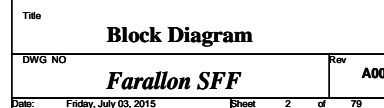
[illegible]

The diagram illustrates the Intel Skylake SoC architecture and its connections to various components. The central component is the **Intel Skylake SoC**, which is connected to several key blocks:

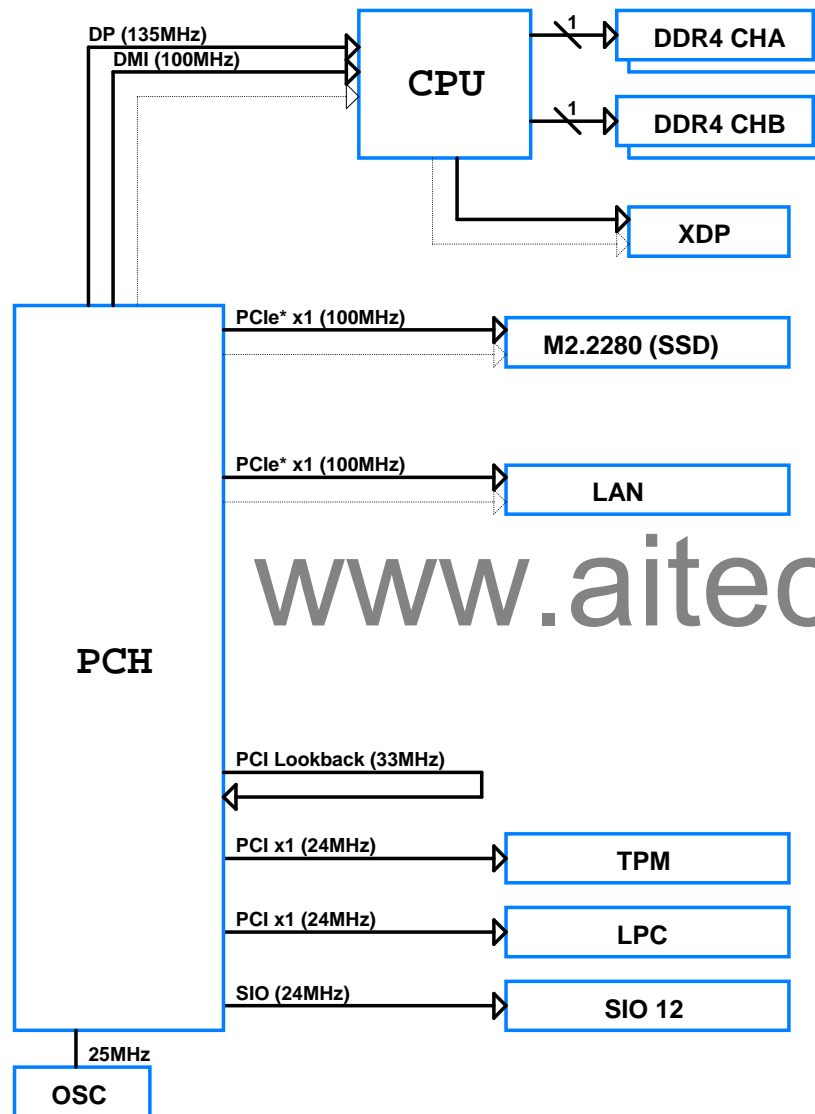
- Intel Skylake Socket**: Connected to the SoC via **QPI** and **PCIe** interfaces. It is further connected to:
 - DDR3 DIMM 1/3** and **DDR3 DIMM 2/4** via **DDR3 QIM** and **DDR3 QIM** interfaces.
 - Intel G-SNA 03** via **PCIe** interface.
 - Realtek ALC3204** via **I2S** interface.
 - SPI Flash (64M128Mb)** via **SPI** interface.
 - Intel I/O** via **SPI** interface.
- Intel PCH-H Q170**: Connected to the SoC via **QPI** and **PCIe** interfaces. It is further connected to:
 - Front USB 2.0 x2** and **Front USB 2.0 x2 w/USB Powershare** via **USB 2.0** and **USB 2.0** interfaces.
 - SA/TA 2.0 Ports x3** via **SA/TA 2.0** interface.
 - PC/EX4 Slot** via **PCIe** interface.
 - CD/DVD** and **System FAN** via **QPI** interface.
 - Serial I2C** via **SPI** interface.
- Intel I/O**: Connected to the SoC via **SPI** interface. It is further connected to:
 - Front Audio x1 (16bit 19.2k)** and **Rear Audio x1 (16bit 19.2k)** via **I2S** interface.
 - Internal Speaker Connector** via **I2S** interface.

The diagram also shows various external ports and components connected to the SoC:


- HDMI Port**, **Display Port**, **Display Port**, **PCIe x16 Slot**, and **VGA Port CONN** are connected to the SoC via **DP 1.0**, **DP 1.0**, **DP 1.0**, **PCIe x16**, and **DP** interfaces.
- Rear USB 3.0 x4** is connected via **USB 3.0** interface.
- Rear USB 2.0 x2 w/Smart power-on** is connected via **USB 2.0** interface.
- Front USB 2.0 x2** and **Front USB 2.0 x2 w/USB Powershare** are connected via **USB 2.0** interface.
- SA/TA 2.0 Ports x3** are connected via **SA/TA 2.0** interface.
- PC/EX4 Slot** is connected via **PCIe** interface.
- CD/DVD** and **System FAN** are connected via **QPI** interface.
- Serial I2C** is connected via **SPI** interface.

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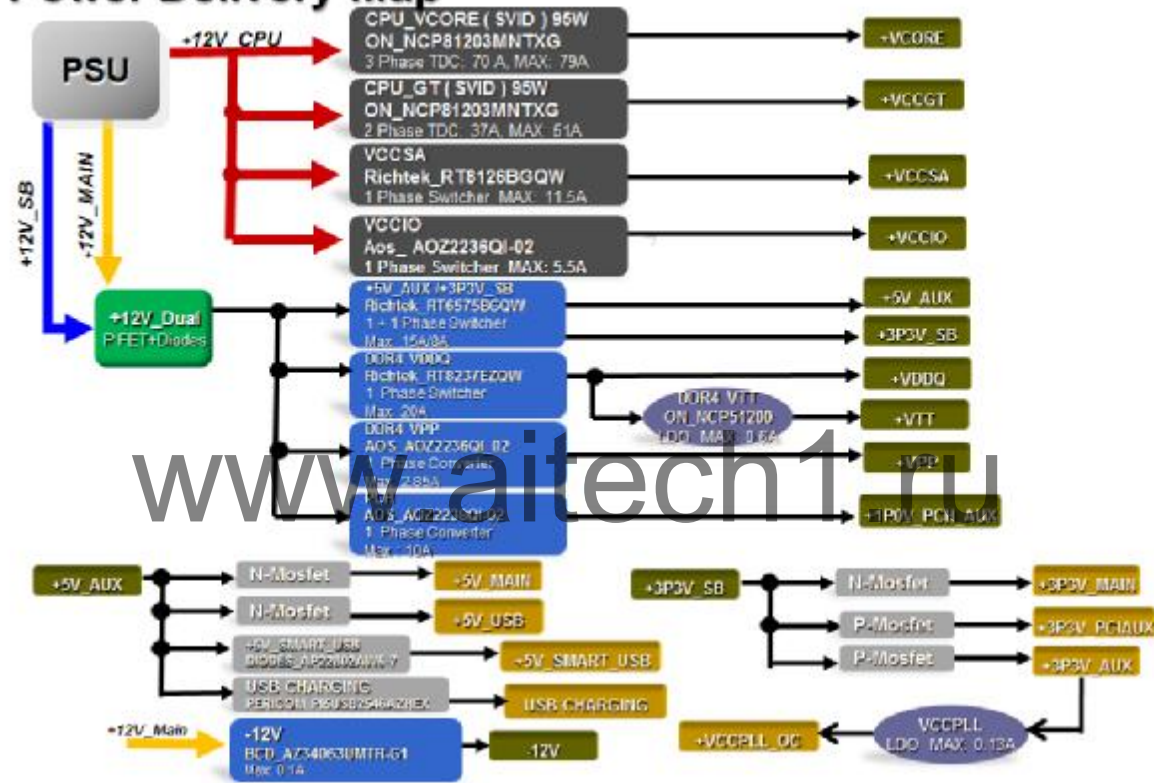
Clock Diagram




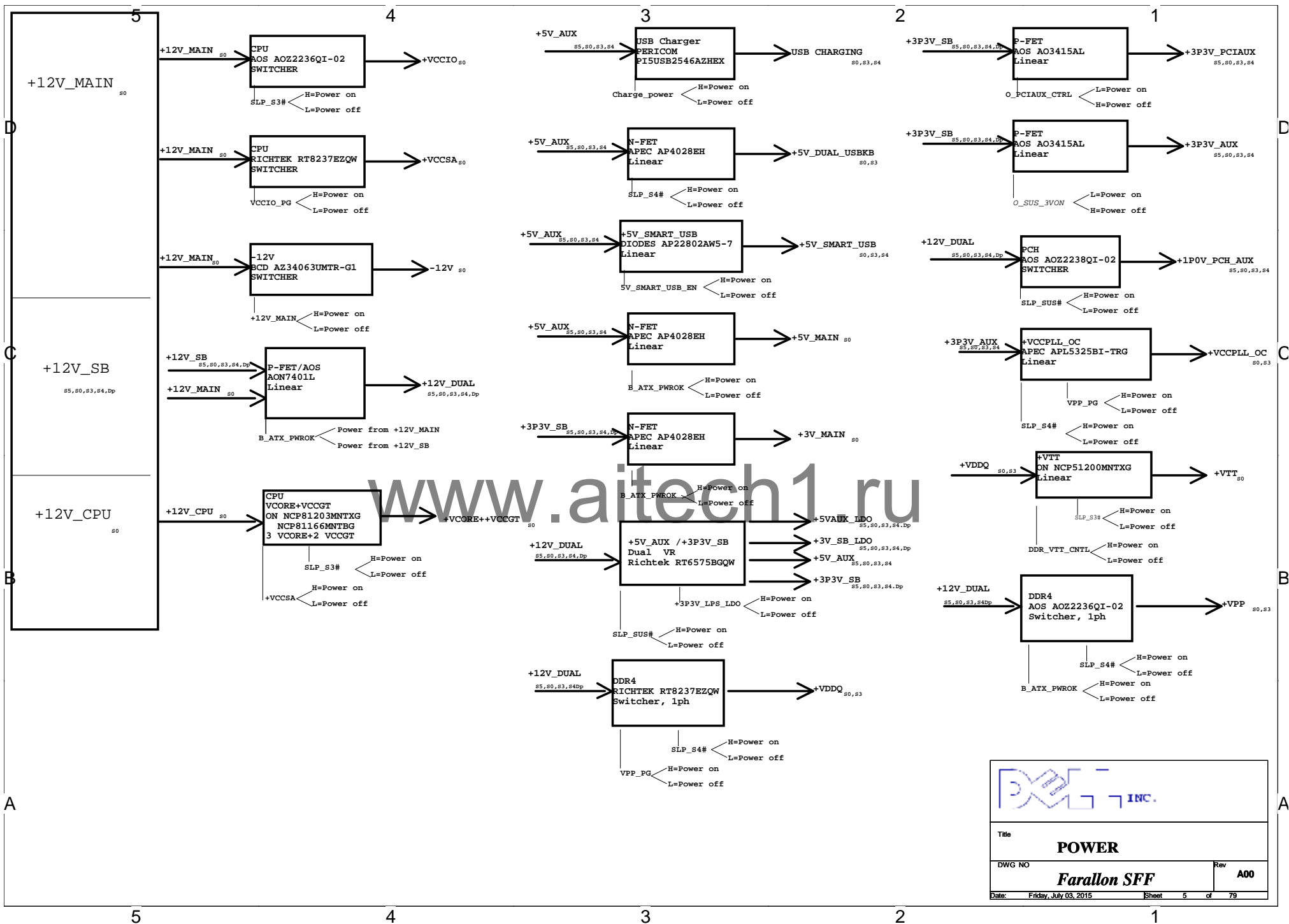
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Title CLOCKS		
DWG NO Farallon SFF	Rev A00	
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Power Delivery Map



	
Title POWER	
DWG NO Farallon SFF	Rev A00
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Title		
POWER		
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Serial	Usage	Where (Example)	Comments															
			This originates from a needs assessment paper.															
			This field defines the detection of anomalies within the data stream. It ranges from 0 (no detection) to 4.0 (2.0 Periodic or 4.0 Irregular Check Response - CRD) (2.0/4.0/CRD). This entry is used in combination with the CRD condition in the following table.															
			<table border="1"> <thead> <tr> <th>CRD</th><th>CRD</th><th>Result (CRD)</th></tr> </thead> <tbody> <tr> <td>0</td><td>1</td><td>Normal</td></tr> <tr> <td>1</td><td>2</td><td>Response</td></tr> <tr> <td>1</td><td>3</td><td>CRD (check)</td></tr> <tr> <td>0</td><td>0</td><td>CRD</td></tr> </tbody> </table>	CRD	CRD	Result (CRD)	0	1	Normal	1	2	Response	1	3	CRD (check)	0	0	CRD
CRD	CRD	Result (CRD)																
0	1	Normal																
1	2	Response																
1	3	CRD (check)																
0	0	CRD																
CRD/CRD + CRD	CRD/CRD/CRD L/C (CRD)	Where value of CRD																
			<p>NOTES</p> <ol style="list-style-type: none"> The status pattern is created after CRD/CRD/CRD. CRD/CRD/CRD is created after the status pattern is created. The CRD/CRD/CRD is created after the status pattern is created. CRD/CRD/CRD is created after the status pattern is created. The CRD/CRD/CRD is created after the status pattern is created. CRD/CRD/CRD is created after the status pattern is created. The CRD/CRD/CRD is created after the status pattern is created. 															

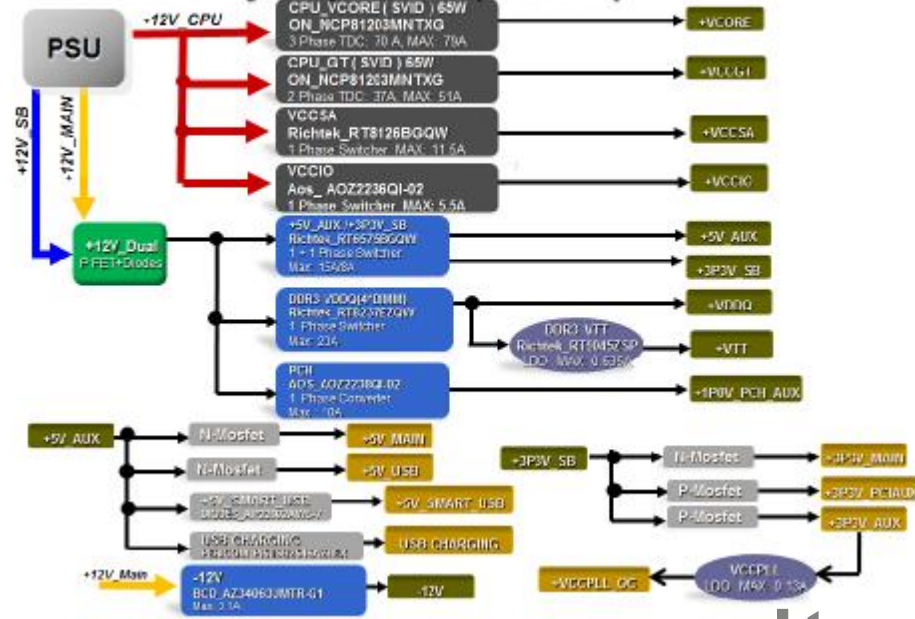
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Rev

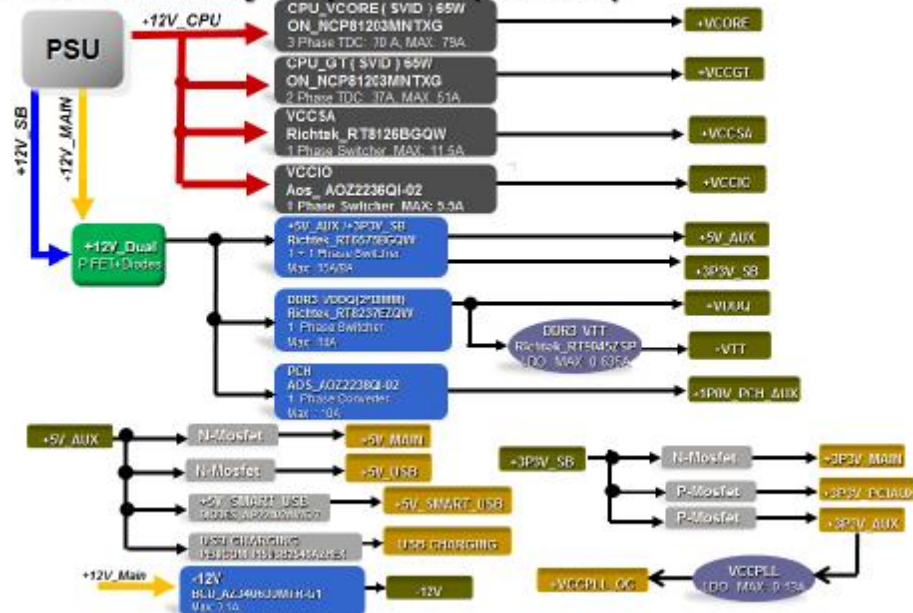
A00

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Power Delivery Map DDR3(4*DIMM)




Power Delivery Map DDR3(2*DIMM)



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Title		
Interrupt & PME		
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20140520 Need check Debug port PDG

20140519 Follow CRB0.5 and PDG0.7

Need to check.

Intel MCP XDP Debug Connector

PREQ# and PRDY# MUST be routed in this order: Debug Port -> CPU -> PCH-H.
place R148, R149 close to CPU

20140520 Follow CRB0.5 and PDG0.7

CRB is dummy R148, R149
PDG is Pop R148, R149

20140520 Follow CRB0.5 and PDG0.7

Need to connect to PCH JTAG pin

20140519 Follow
CRB0.5 and PDG0.7

Note :
VCCST Power Gating (Q1) implemented : XDP_PRESENT# need connect to Q1.G with a inverse logic.


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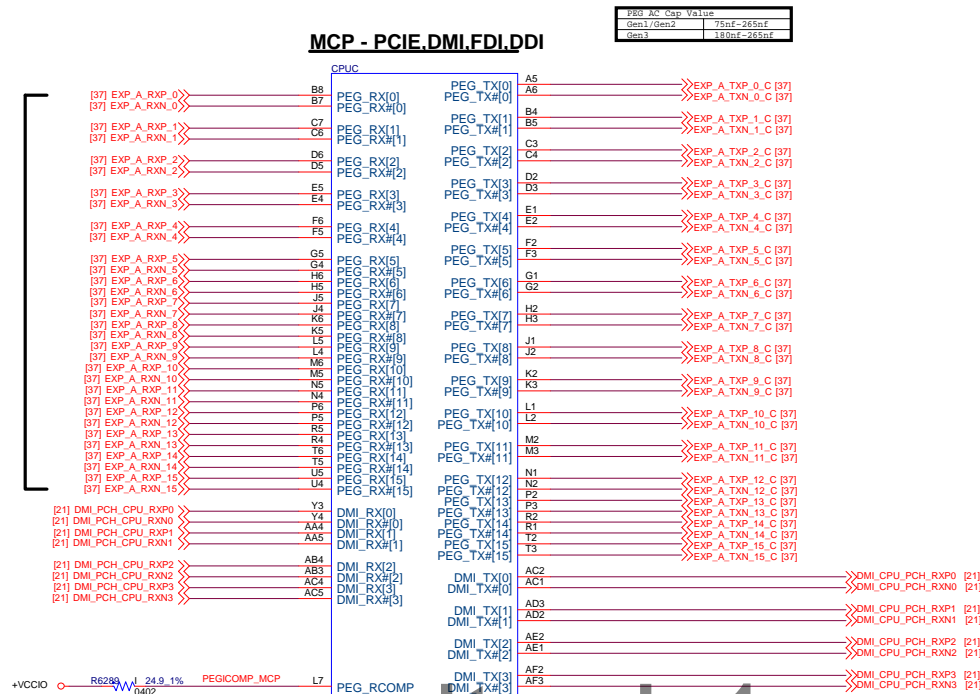


Title	
CPU-XDP	
DWG NO	Rev
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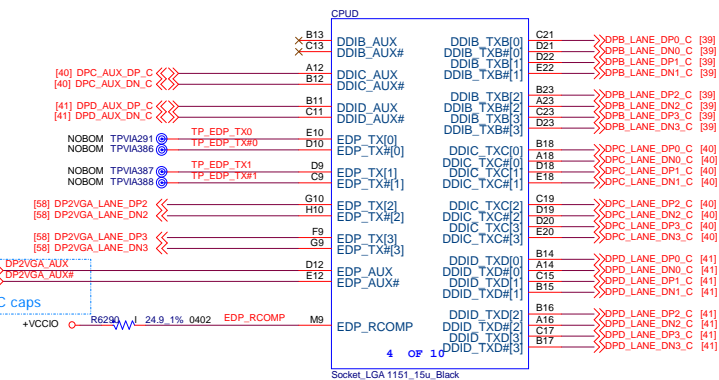
FOXCONN CONFIDENTIAL

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Title DDR3 CHANEL A/B	
DWG NO Farallon SFF	Rev A00
Date: Friday, July 03, 2015 Sheet 11 of 79	



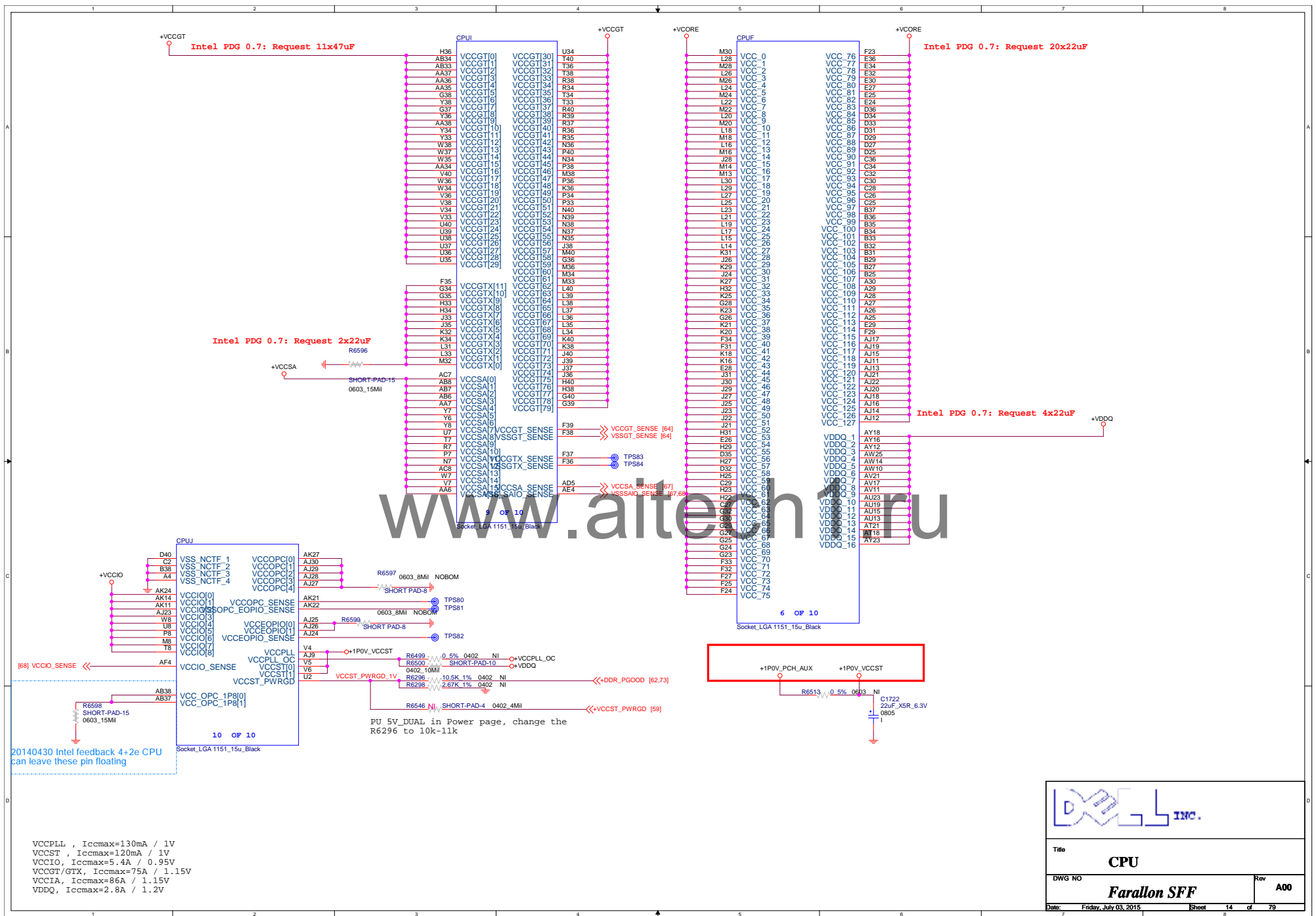
Pin 40402: PEG2B, 24.9 1%, PEGCOMP_MCP, L7, PEG_RCOMP, DMI_TX[3], DMI_TX#(3), AF3, XMI_CPU_PU, XMI_CPU_PU. Socket: LGA 1151, 15u, Black.

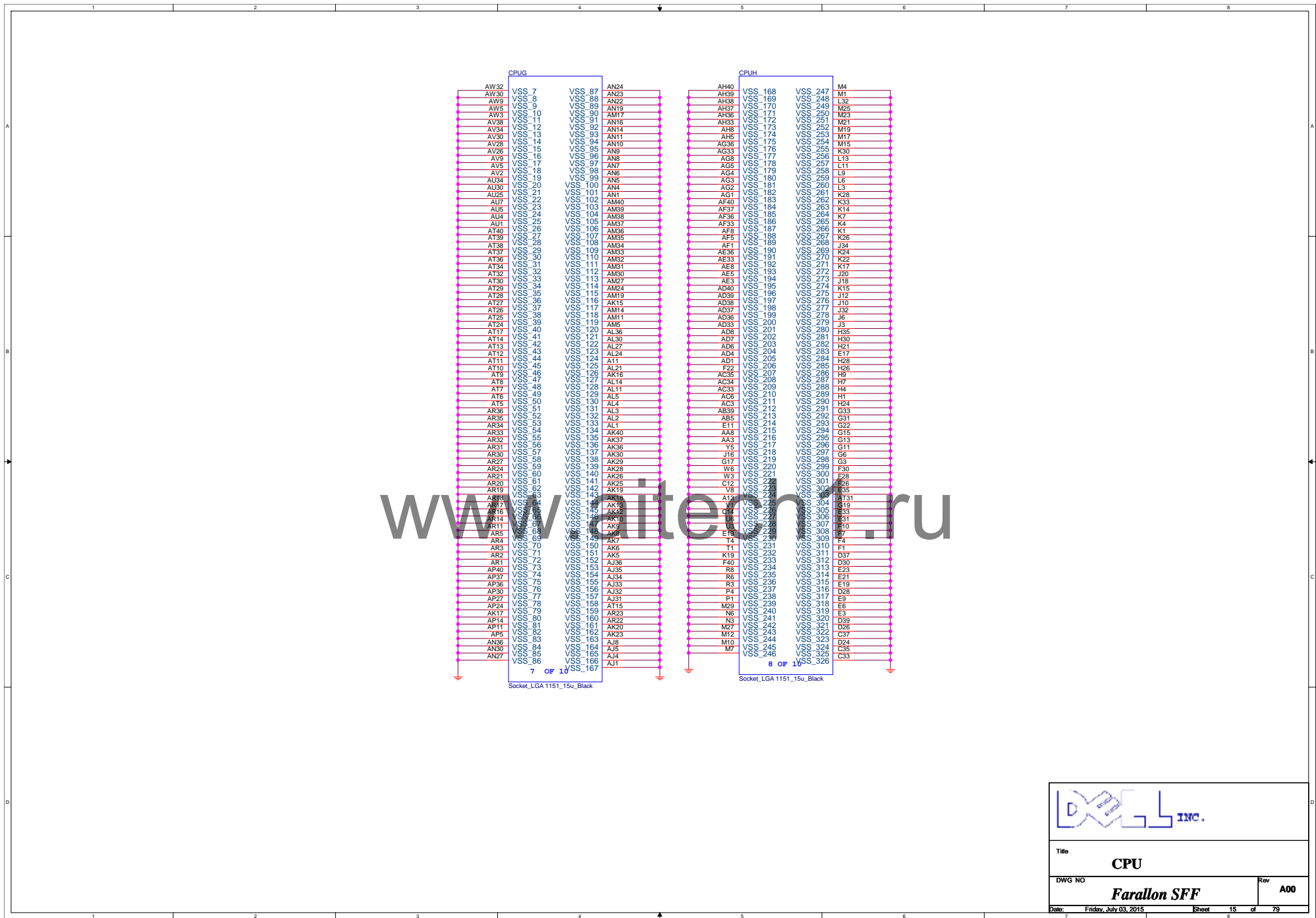



Processor PCI Express® Compensation Signal Routing Guidelines					
Parameter	Units	Trace width	Trace spacing to other signals	Routing Length	Resistance
PEG_RCOMP	mils	12	15	400	
Resistor	ohm				24.9+-1%



Title		CPU	
DWG NO		Rev	
<i>Farallon SFF</i>		A00	
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Title	
CPU	
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Intel PCH XDP Debug Connector

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Project	
Spitfire	V
Scorpion	V
Toledo	V

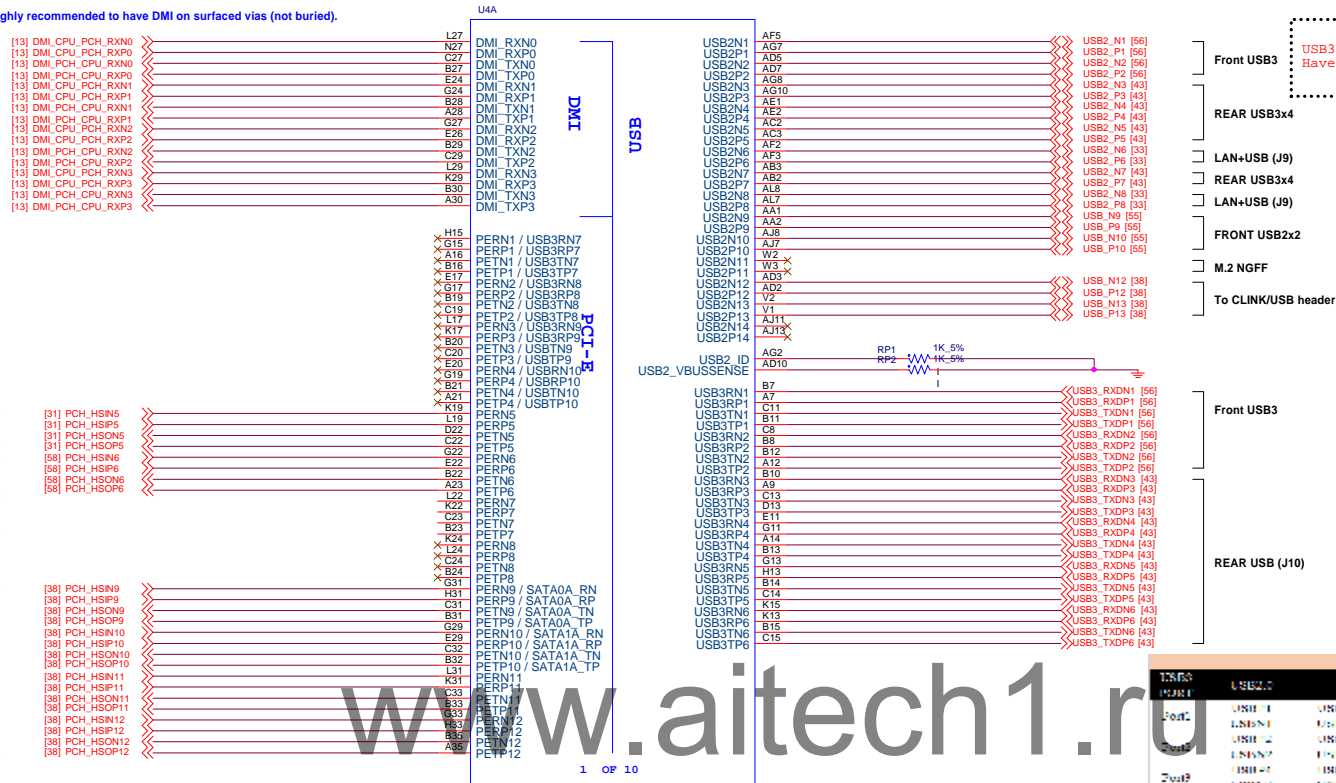
	
Title CPU	
DWG NO Farallon SFF	Rev A00
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It is highly recommended to have DMI on surfaced vias (not buried).



USB3 and USB2 port mapping is not clear in PDG. Have to check again if Intel releases new PDG.

ARD1.06 PCH I/O Port Mapping

Port#	Signal	Interface	Device	Port#	Signal	Interface	Device
1	USB3A1	USB3	Front USB3 conn.	1	USB3A1	USB3	Front USB3 conn.
2	USB3A2	USB3	Front USB3 conn.	2	USB3A2	USB3	Front USB3 conn.
3	USB3A3	USB3	Rear USB3 conn.	3	USB3A3	USB3	Rear USB3 conn.
4	USB3A4	USB3	Rear USB3 conn.	4	USB3A4	USB3	Rear USB3 conn.
5	USB3A5	USB3	Rear USB3 conn.	5	USB3A5	USB3	Rear USB3 conn.
6	USB3A6	USB3	Rear USB3 conn.	6	USB3A6	USB3	Rear USB3 conn.
7	USB3A7	USB3	Rear USB3 conn.	7	USB3A7	USB3	Rear USB3 conn.
8	USB3A8	USB3	Rear USB3 conn.	8	USB3A8	USB3	Rear USB3 conn.
9	USB3A9	USB3	Rear USB3 conn.	9	USB3A9	USB3	Rear USB3 conn.
10	USB3A10	USB3	Rear USB3 conn.	10	USB3A10	USB3	Rear USB3 conn.
11	PCIe1A0	PCIe	NIC	11	PCIe1A0	PCIe	NIC
12	PCIe1A1	PCIe	NIC	12	PCIe1A1	PCIe	NIC
13	PCIe1A2	PCIe	NIC	13	PCIe1A2	PCIe	NIC
14	PCIe1A3	PCIe	NIC	14	PCIe1A3	PCIe	NIC
15	PCIe1A4	PCIe	NIC	15	PCIe1A4	PCIe	NIC
16	PCIe1A5	PCIe	NIC	16	PCIe1A5	PCIe	NIC
17	PCIe1A6	PCIe	NIC	17	PCIe1A6	PCIe	NIC
18	PCIe1A7	PCIe	NIC	18	PCIe1A7	PCIe	NIC
19	PCIe1A8	PCIe	NIC	19	PCIe1A8	PCIe	NIC
20	PCIe1A9	PCIe	NIC	20	PCIe1A9	PCIe	NIC
21	PCIe1A10	PCIe	NIC	21	PCIe1A10	PCIe	NIC
22	PCIe1A11	PCIe	NIC	22	PCIe1A11	PCIe	NIC
23	PCIe1A12	PCIe	NIC	23	PCIe1A12	PCIe	NIC
24	PCIe1A13	PCIe	NIC	24	PCIe1A13	PCIe	NIC
25	PCIe1A14	PCIe	NIC	25	PCIe1A14	PCIe	NIC
26	PCIe1A15	PCIe	NIC	26	PCIe1A15	PCIe	NIC
27	PCIe1A16	PCIe	NIC	27	PCIe1A16	PCIe	NIC
28	PCIe1A17	PCIe	NIC	28	PCIe1A17	PCIe	NIC
29	PCIe1A18	PCIe	NIC	29	PCIe1A18	PCIe	NIC
30	PCIe1A19	PCIe	NIC	30	PCIe1A19	PCIe	NIC
31	PCIe1A20	PCIe	NIC	31	PCIe1A20	PCIe	NIC

USB2 Port	Pin Name	Pin Type	Signal Name	Signal Type	Signal Name	Signal Type
1	USB2A1	USB2	USB2A1	USB2	USB2A1	USB2
2	USB2A2	USB2	USB2A2	USB2	USB2A2	USB2
3	USB2A3	USB2	USB2A3	USB2	USB2A3	USB2
4	USB2A4	USB2	USB2A4	USB2	USB2A4	USB2
5	USB2A5	USB2	USB2A5	USB2	USB2A5	USB2
6	USB2A6	USB2	USB2A6	USB2	USB2A6	USB2
7	USB2A7	USB2	USB2A7	USB2	USB2A7	USB2
8	USB2A8	USB2	USB2A8	USB2	USB2A8	USB2
9	USB2A9	USB2	USB2A9	USB2	USB2A9	USB2
10	USB2A10	USB2	USB2A10	USB2	USB2A10	USB2
11	USB2A11	USB2	USB2A11	USB2	USB2A11	USB2
12	USB2A12	USB2	USB2A12	USB2	USB2A12	USB2
13	USB2A13	USB2	USB2A13	USB2	USB2A13	USB2
14	USB2A14	USB2	USB2A14	USB2	USB2A14	USB2
15	USB2A15	USB2	USB2A15	USB2	USB2A15	USB2
16	USB2A16	USB2	USB2A16	USB2	USB2A16	USB2
17	USB2A17	USB2	USB2A17	USB2	USB2A17	USB2
18	USB2A18	USB2	USB2A18	USB2	USB2A18	USB2
19	USB2A19	USB2	USB2A19	USB2	USB2A19	USB2
20	USB2A20	USB2	USB2A20	USB2	USB2A20	USB2

INC.

Title

PCH

DWG NO

Farallon SFF

Rev

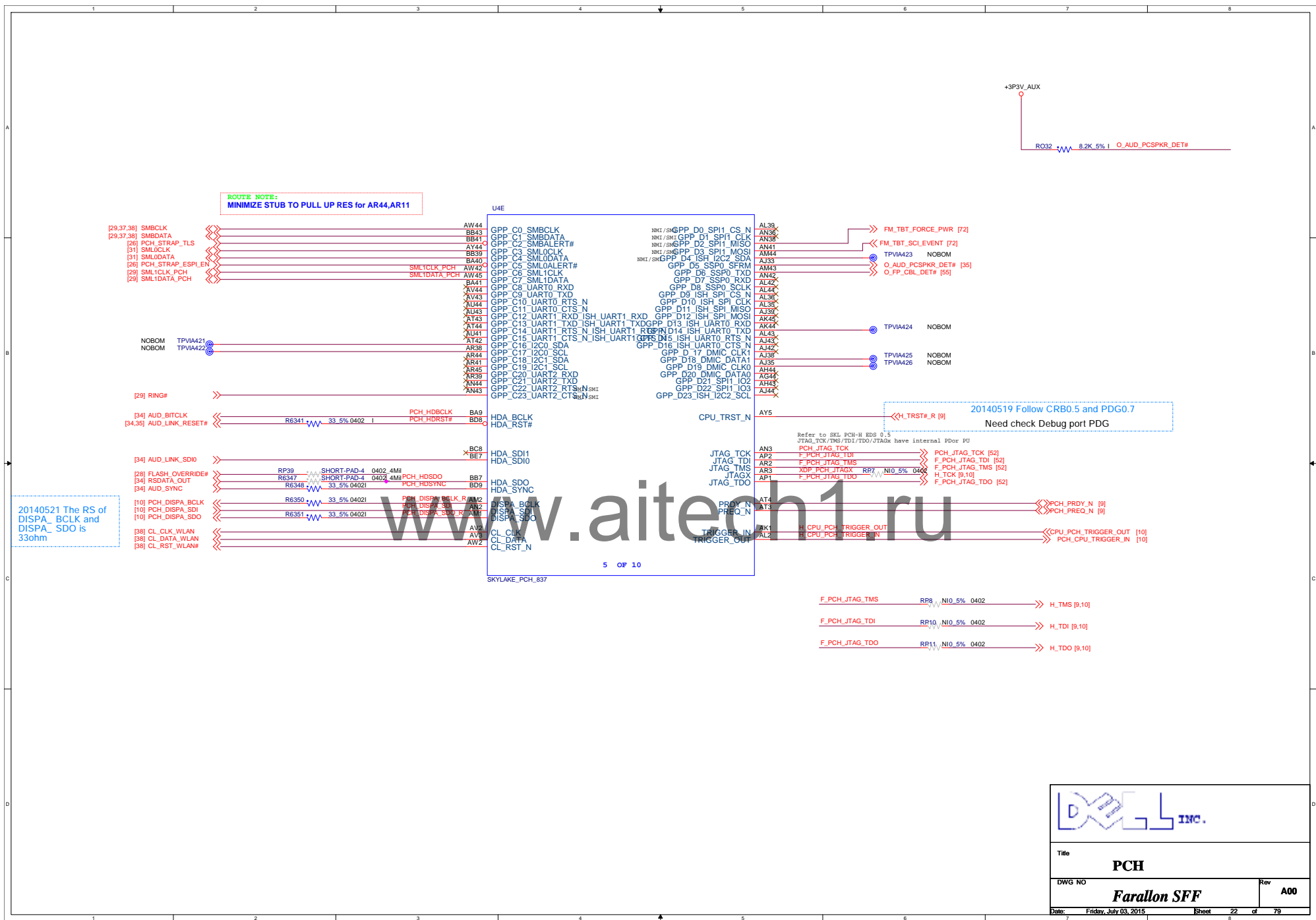
A00

Date

Friday, July 03, 2015

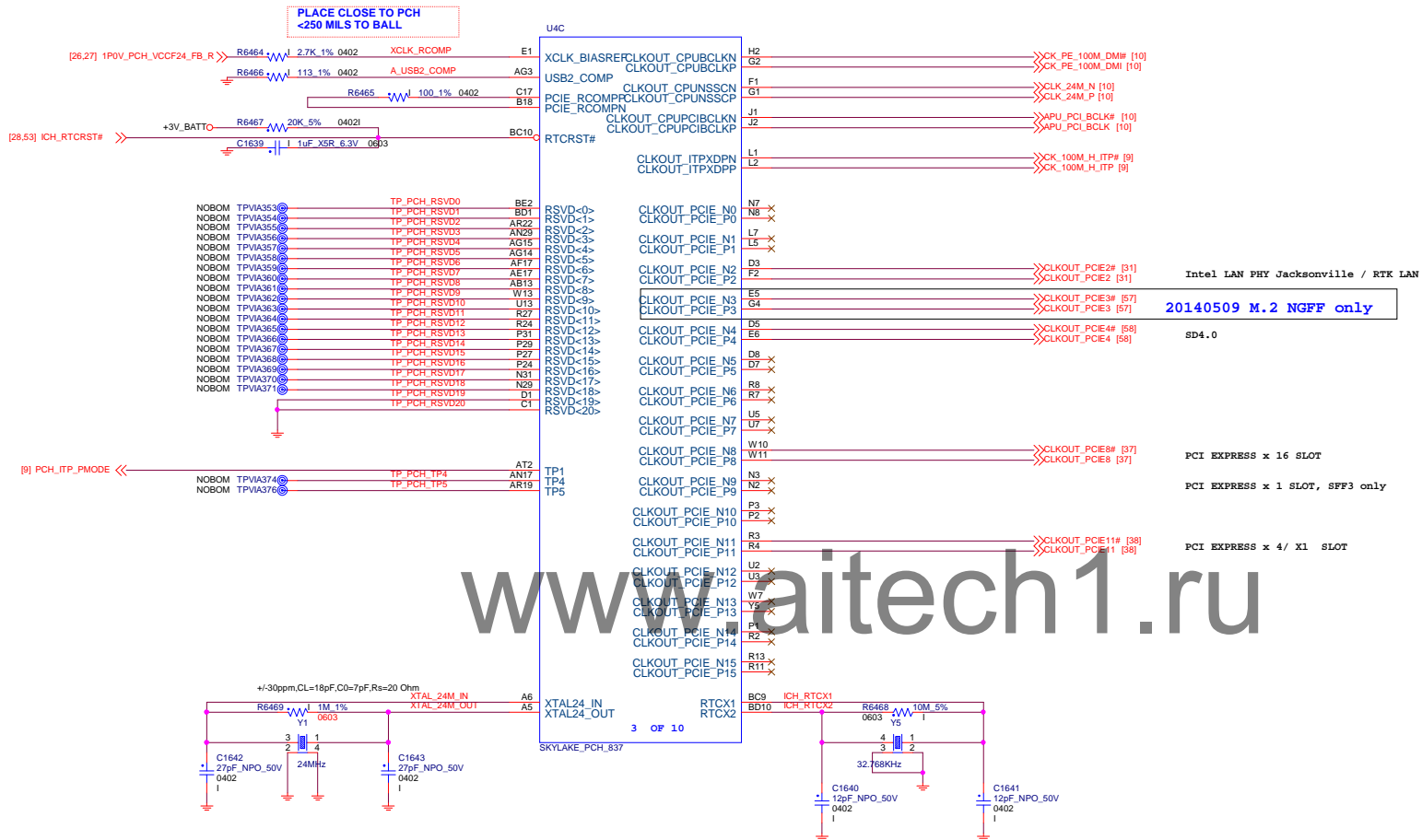
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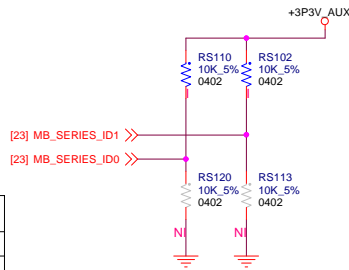
PCH - CLOCK DISTRIBUTION



DEL INC.	
Title PCH	
DWG NO Farallon SFF	Rev A00
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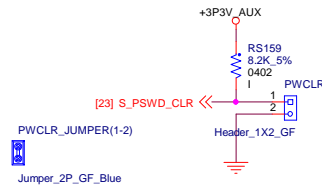
MB series ID

ID1	ID0	Type
0	0	SFF3
0	1	SFF5
1	0	SFF7
1	1	Farallon



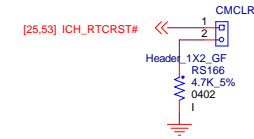
Clear Password

PASSWORD	SHORT : DEFAULT
	OPEN : CLEAR PASSWORD



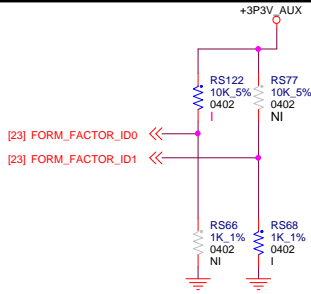
CLR_CMOS

CMOS	SHORT : CLEAR CMOS
	OPEN : DEFAULT

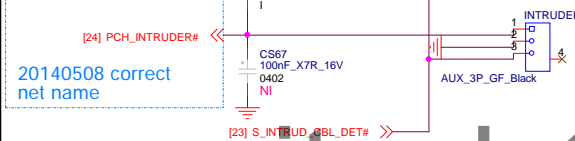


Form Factor ID

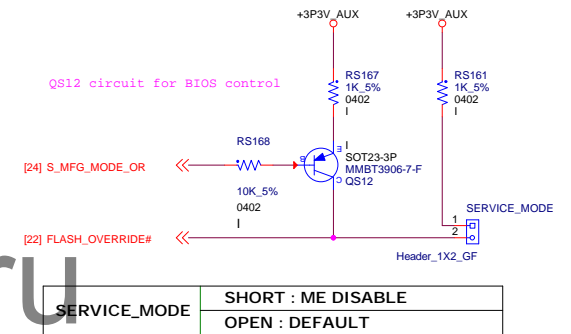
ID1	ID0	Type
1	1	MT
1	0	CT
0	1	SFF
0	0	Micro



Chassis Intruder

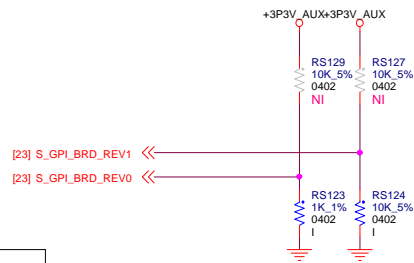


ME Disable (Flash override)



BOARD ID

ID1	ID0	Type
1	1	X02
1	0	X01
0	1	X00
0	0	B00/A00



BEEP

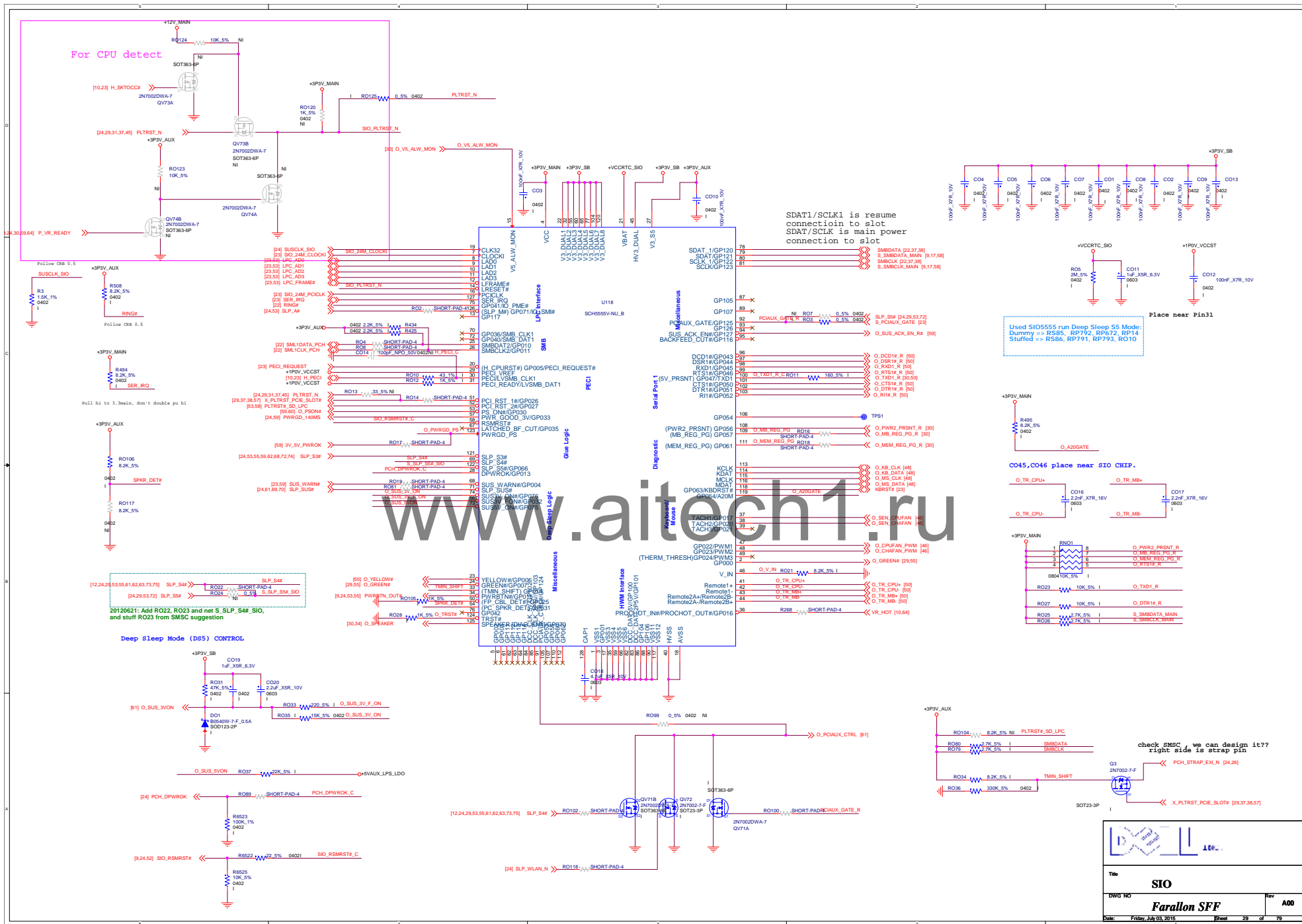
DELTA INC.

Title: **PCH**

DWG NO: **Farallon SFF**

Rev: **A00**

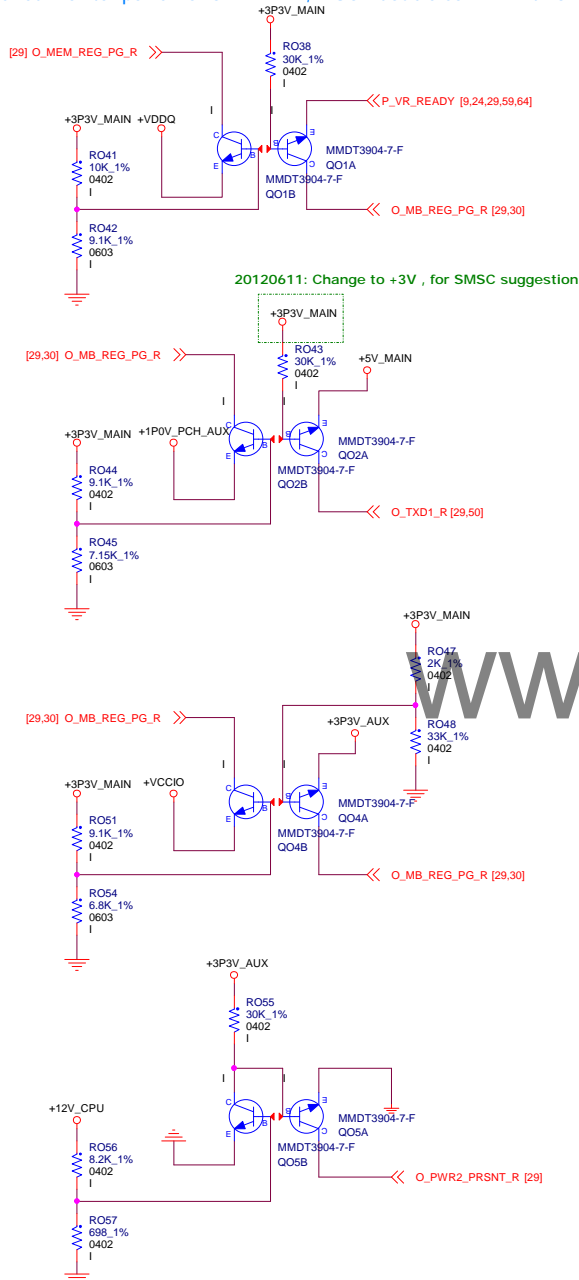
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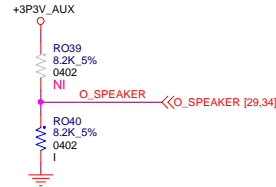
Title		
SIO		
DWG NO	Rev	A00
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5555 PRE-POST DIAG Monitor

20140429 Chained monitor power for SKYLAKE , MUST double confirm with SMSC



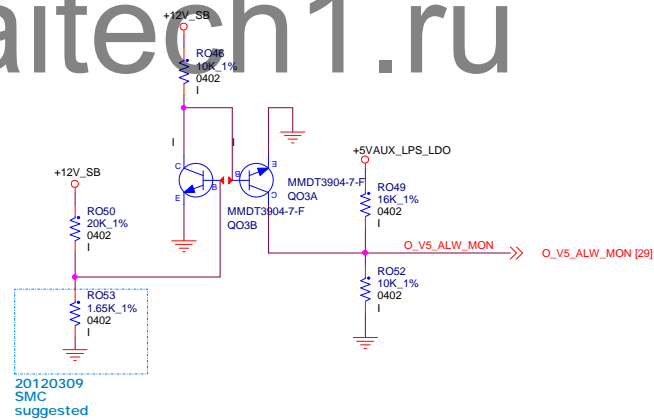
SIO STRAPING



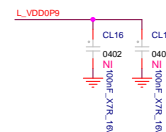
SIO STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	Disable	
PULL LOW	Enable	


SIO5555 V5_ALW Monitor



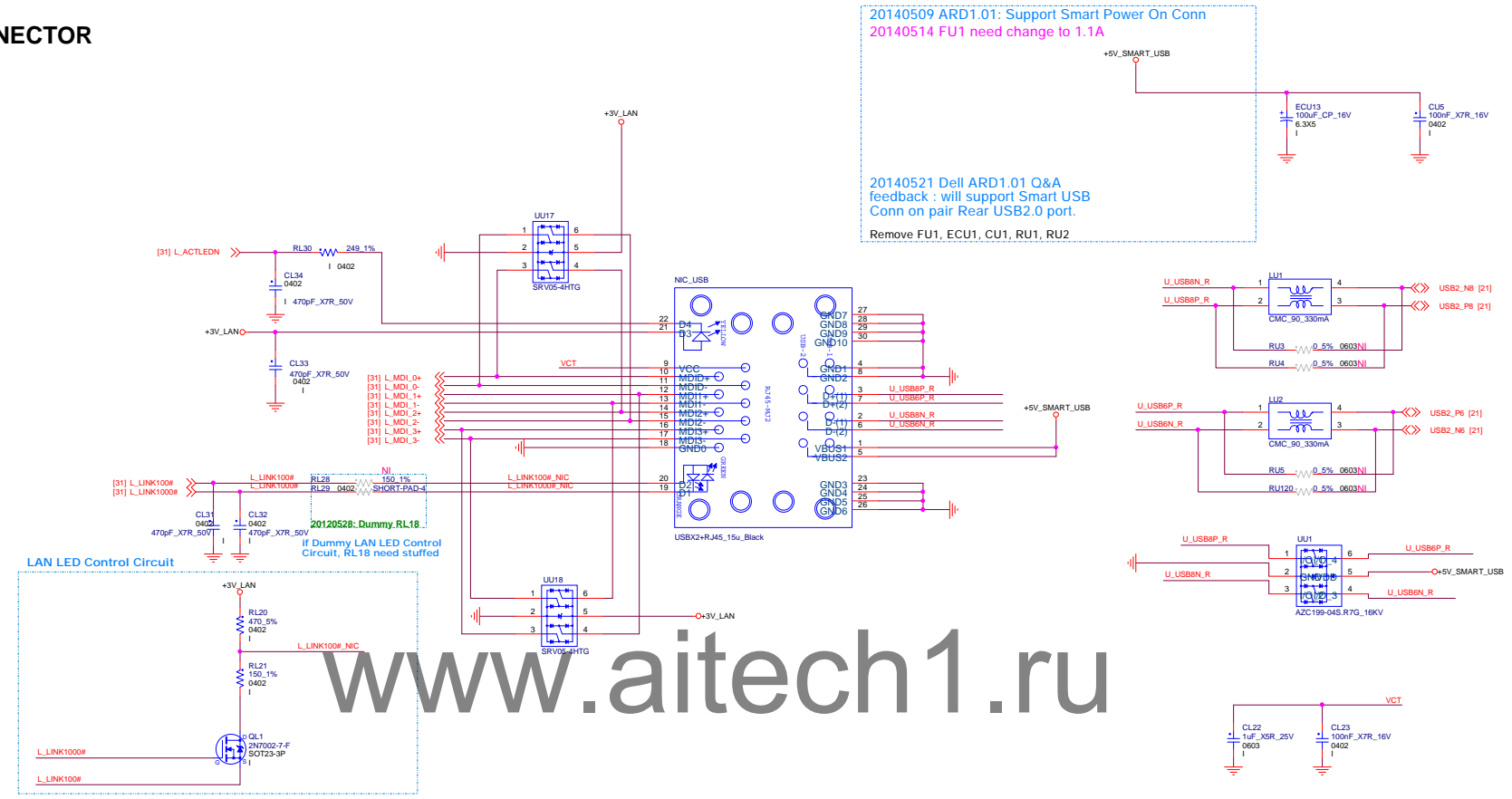
Title	SIO	
DWG NO	Farallon SFF	
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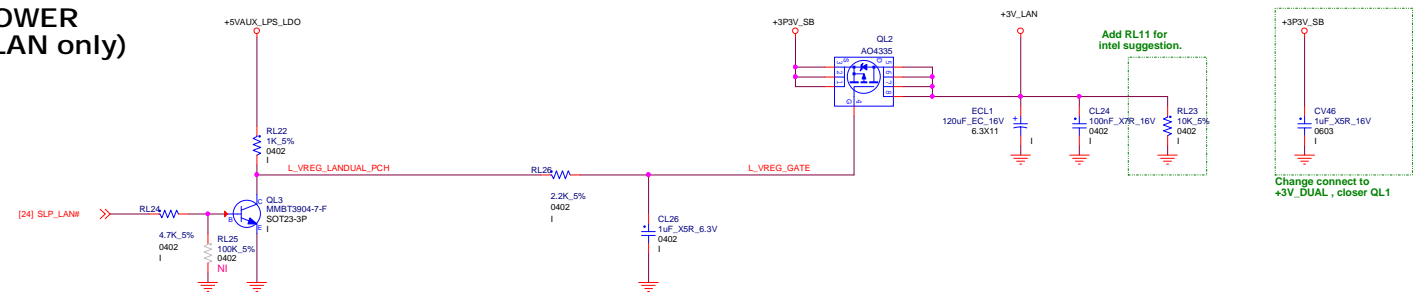
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Title	
LAN	
DWG NO	Rev
Farallon SFF	A00
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LAN CONNECTOR




LAN POWER (Intel LAN only)

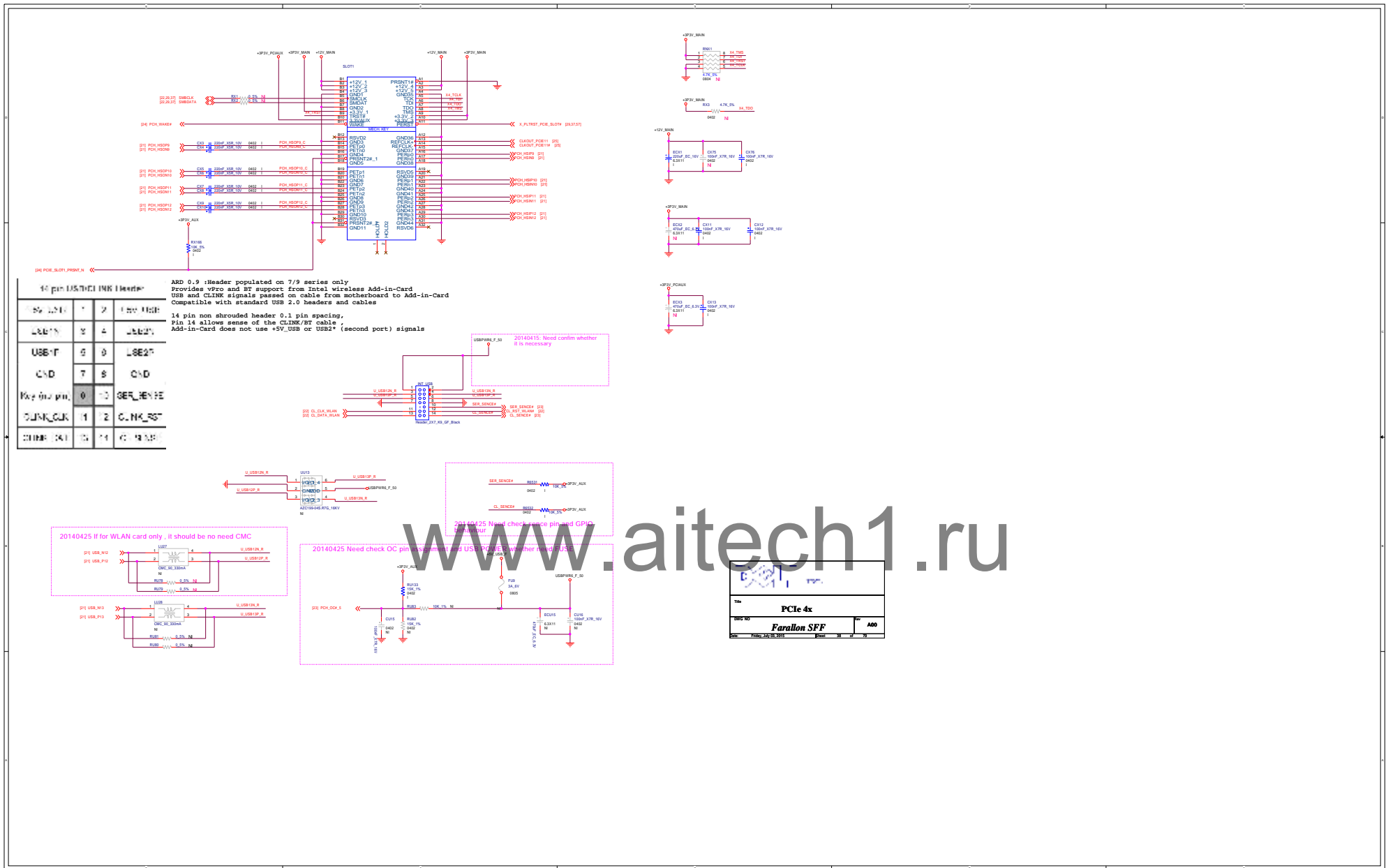


Title		
LAN		
DWG NO		
Farallon SFF		
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Rev		
A00		

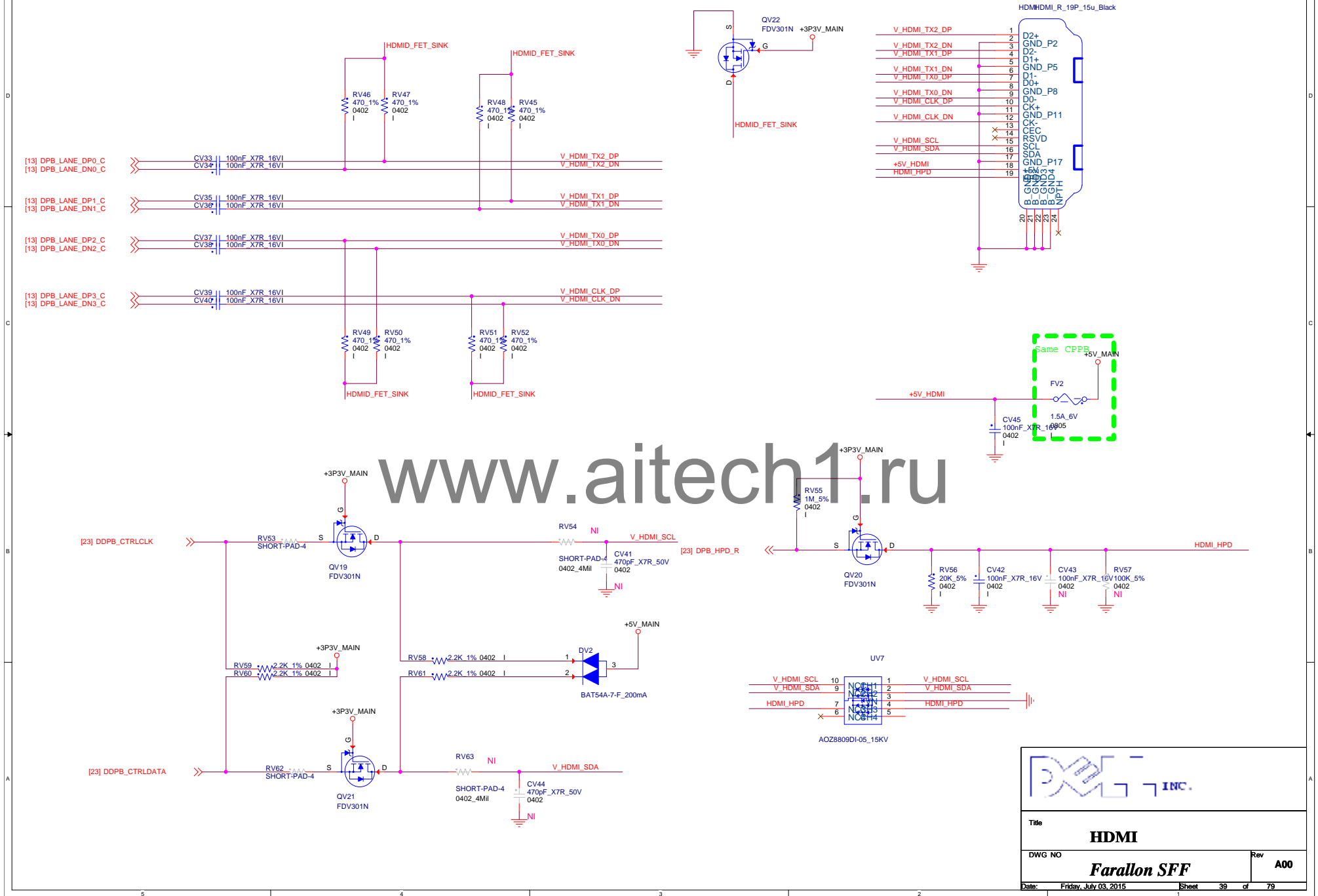
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Title		
PCIe 1x		
DWG NO	Rev	A00
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HDMI1 --> Port B



		
Title		
HDMI		
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DP --> Port D

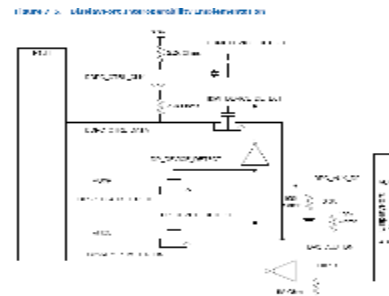
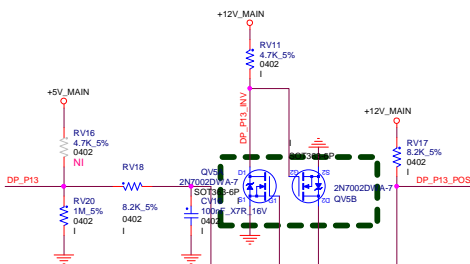
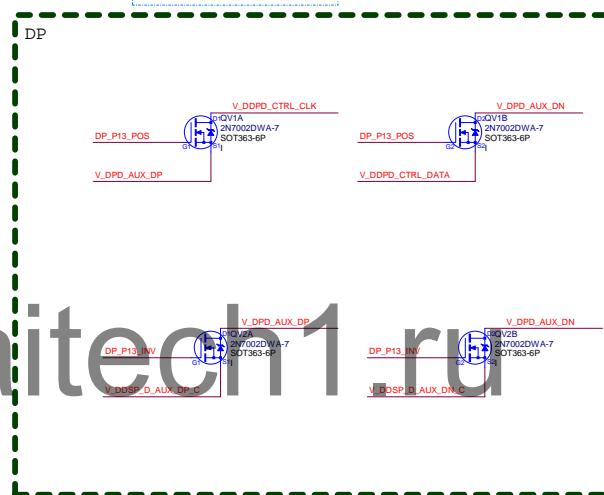
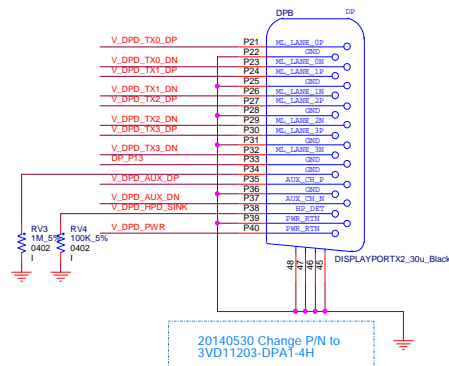
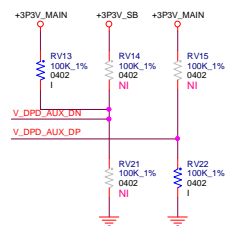
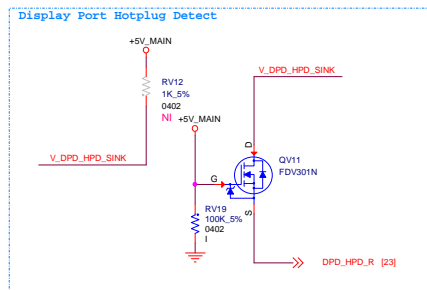
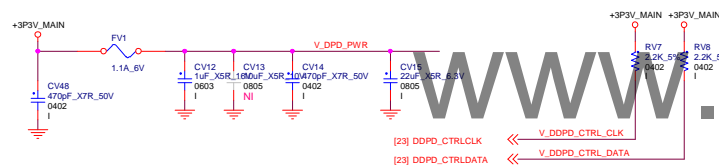
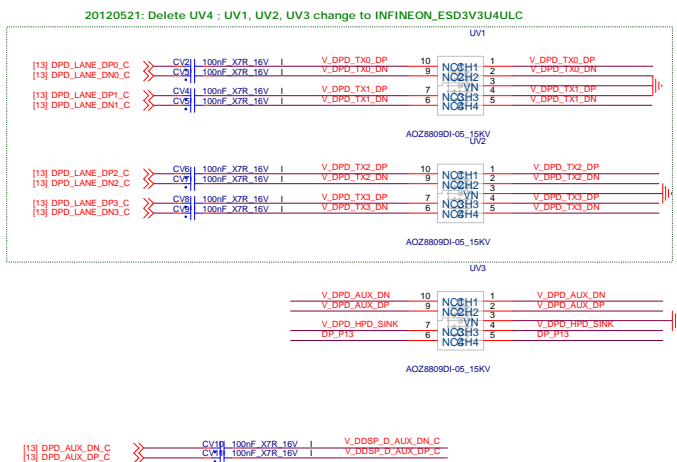
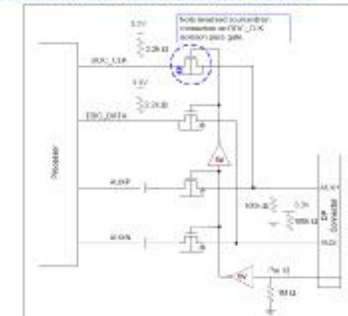
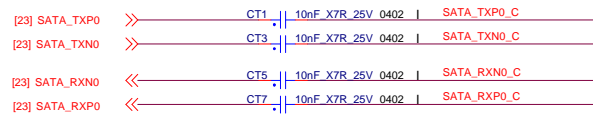
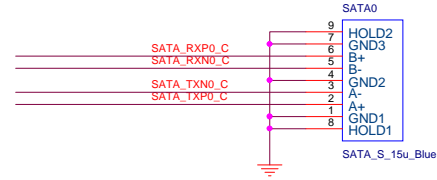


Figure 5-11. DisplayPort® Auxiliary Channel Dual Mode Support Properties Dialog

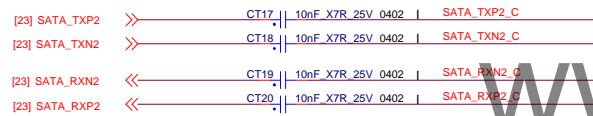
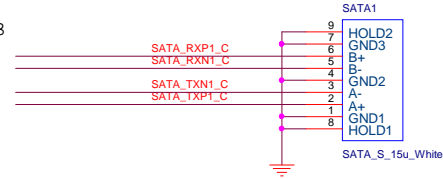




Blue SATA3

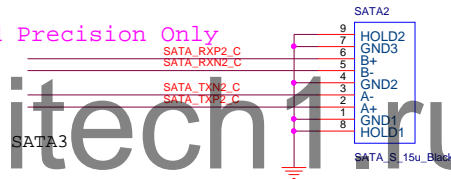


white ODD SATA3




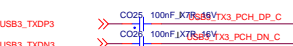
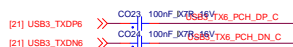
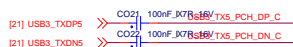
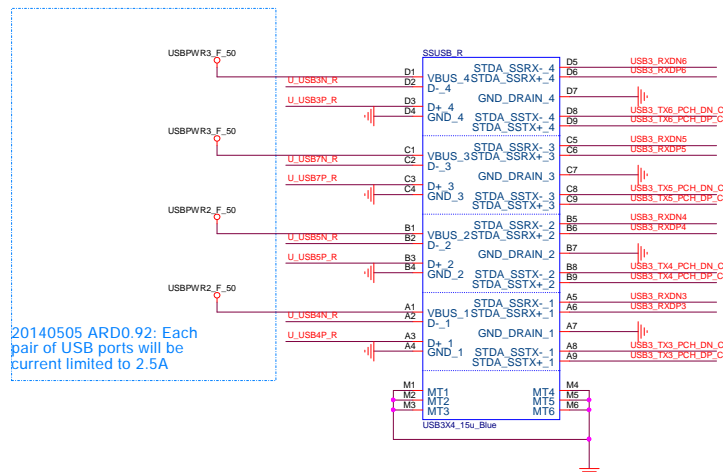
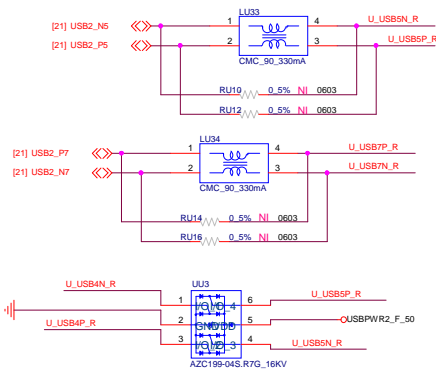
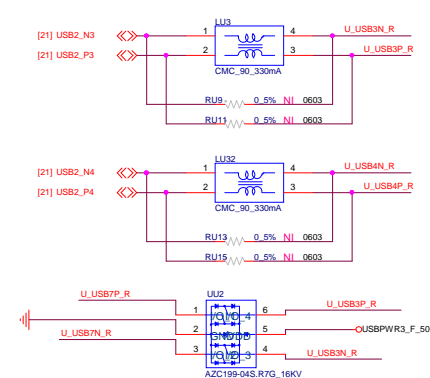
SFF7/5 and Precision Only

Black SATA3

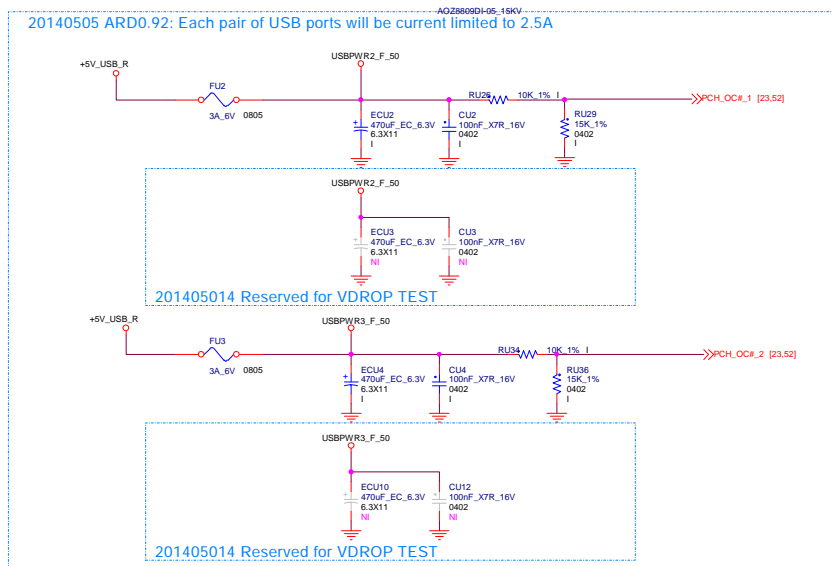


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Title	
SATA Conn	
DWG NO	Rev
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www.aitech1.ru



		Title	
		Rear USB	
DWG NO		Rev	
Farallon SFF		A00	
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www.aitech1.ru

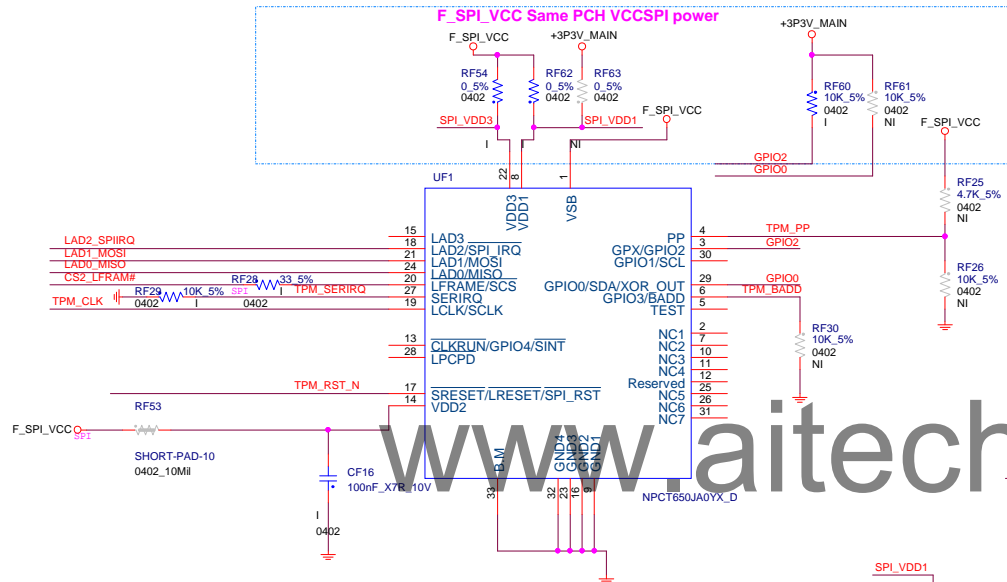
	
Title	
Rear USB	
DWG NO	Rev
Farallon SFF	A00
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Sheet 44 of 79	

Trusted Computing Support

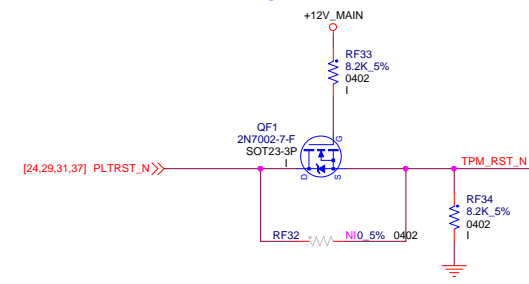
HW Low Power Mode	RF62	RF63	RF60
Support	Un-stuff	Stuff	Stuff
Not support	Stuff	Un-stuff	Un-stuff

Nuvoton NPCT650JAAYX - 2.0 NPCT650JA0YX - 1.2

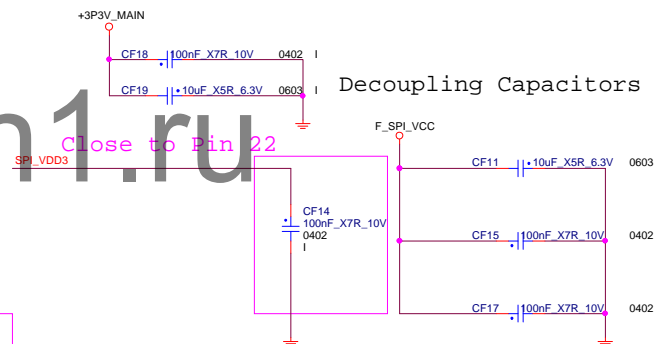
F_SPL_VCC Same PCH VCCSPI power



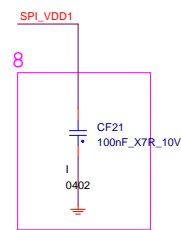
20140508 Follow Dell D serials design




Decoupling Capacitors

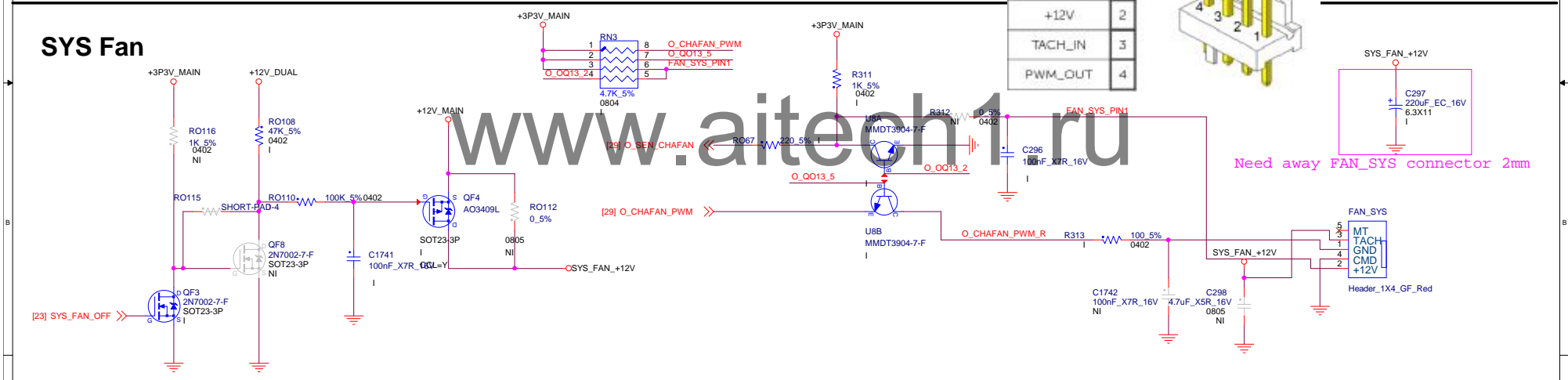


Close to Pin 8



NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- CF17 is required only for the NPCT620/650.


	
Title TPM	
DWG NO Farallon SFF	Rev A00
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[illegible]

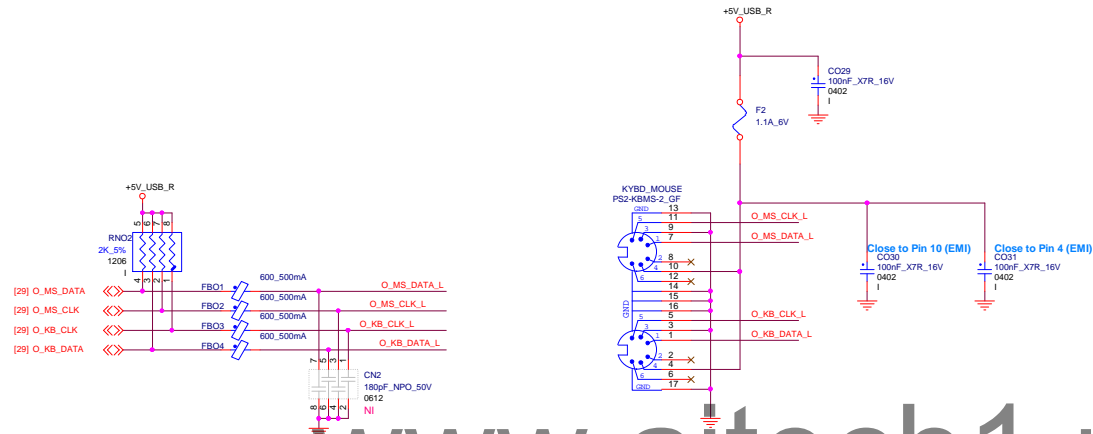
The figure shows a technical drawing of a label. The label is rectangular with a width of 5 units and a height of 4 units. It is divided into two main sections. The left section is a rectangle with a width of 1 unit and a height of 1 unit, labeled 'Type_T_PPID_Label'. The right section is a rectangle with a width of 4 units and a height of 1 unit, labeled 'PPID'. Inside the right section, there is a circular feature with a diameter of 1 unit, labeled 'PPID' and 'NI'. The label is shown with a pink border. The drawing is titled 'LABEL' and includes a title block with the following information:

Title		FAN & LABEL	
DWG NO	Rev		A00
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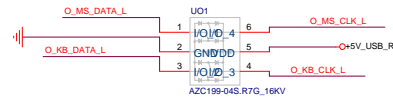
www.aitech1.ru


	
Title PS2 Conn	
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KB/MS




www.aitech1.ru

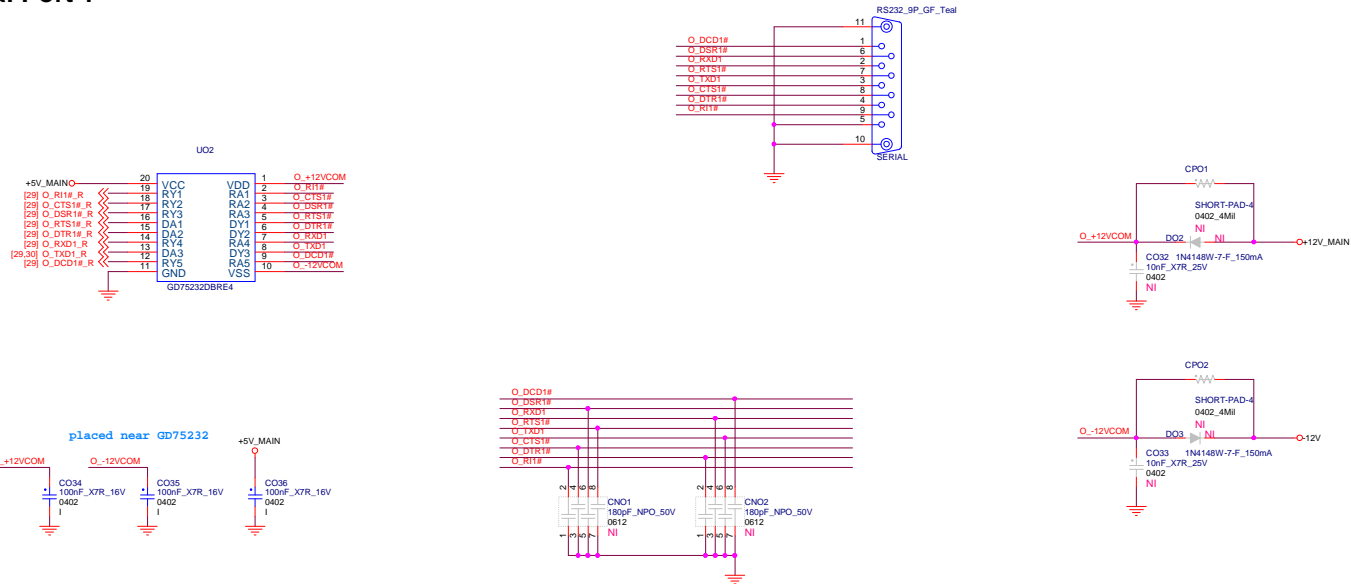


	
Title PS2 Conn	
DWG NO Farallon SFF	Rev A00
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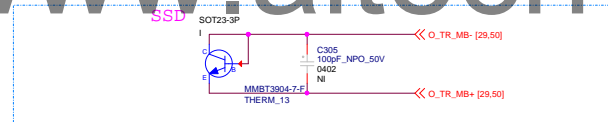
www.aitech1.ru

	
Title Thermal Sensor	
DWG NO Farallon SFF	Rev A00
Date: Friday, July 03, 2015 Sheet 49 of 79	

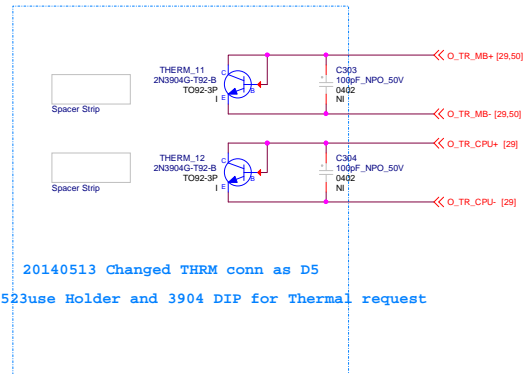
Serial Port 1



www.aitech1.ru



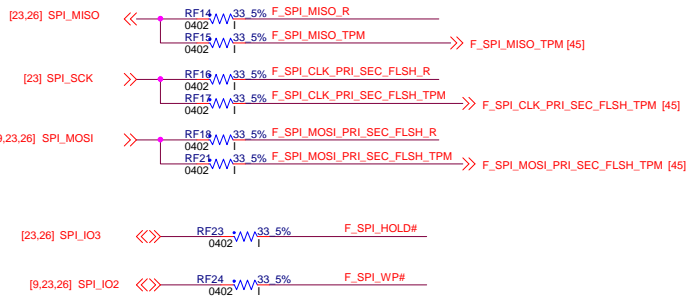
Thermal Header



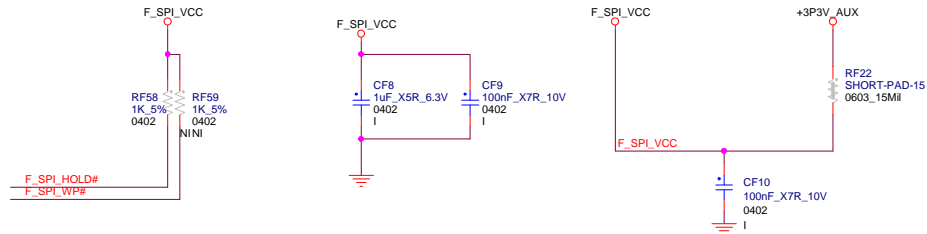
20140513 Changed THRM conn as D5

20040523 use Holder and 3904 DIP for Thermal request

Title		
COM1		
DWG NO	Rev	A00
Farallon SFF		
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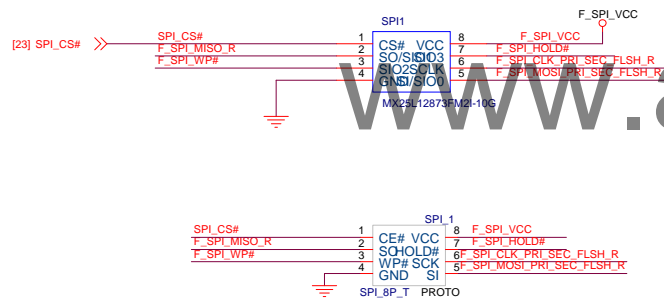
20140506 Follow CRB0.5 and PDG0.7 use +3P3V_ AUX (enabled by SLP_ SUS#) for SPI VCC



SPI_16MB

20140506 ARD0.92 : One SPI FLASH device site on PCB

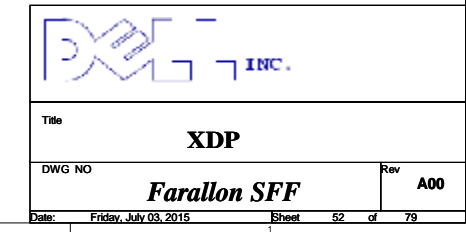
Before RTS, please use DIP

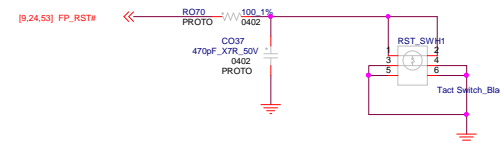
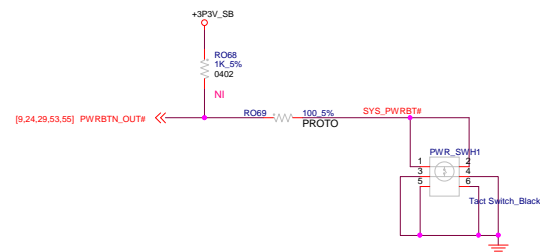


Title		
SPI		
DWG NO		Rev
Farallon SFF		A00
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20140505 Remove Duplicated XDP

XDP Connector - PCH



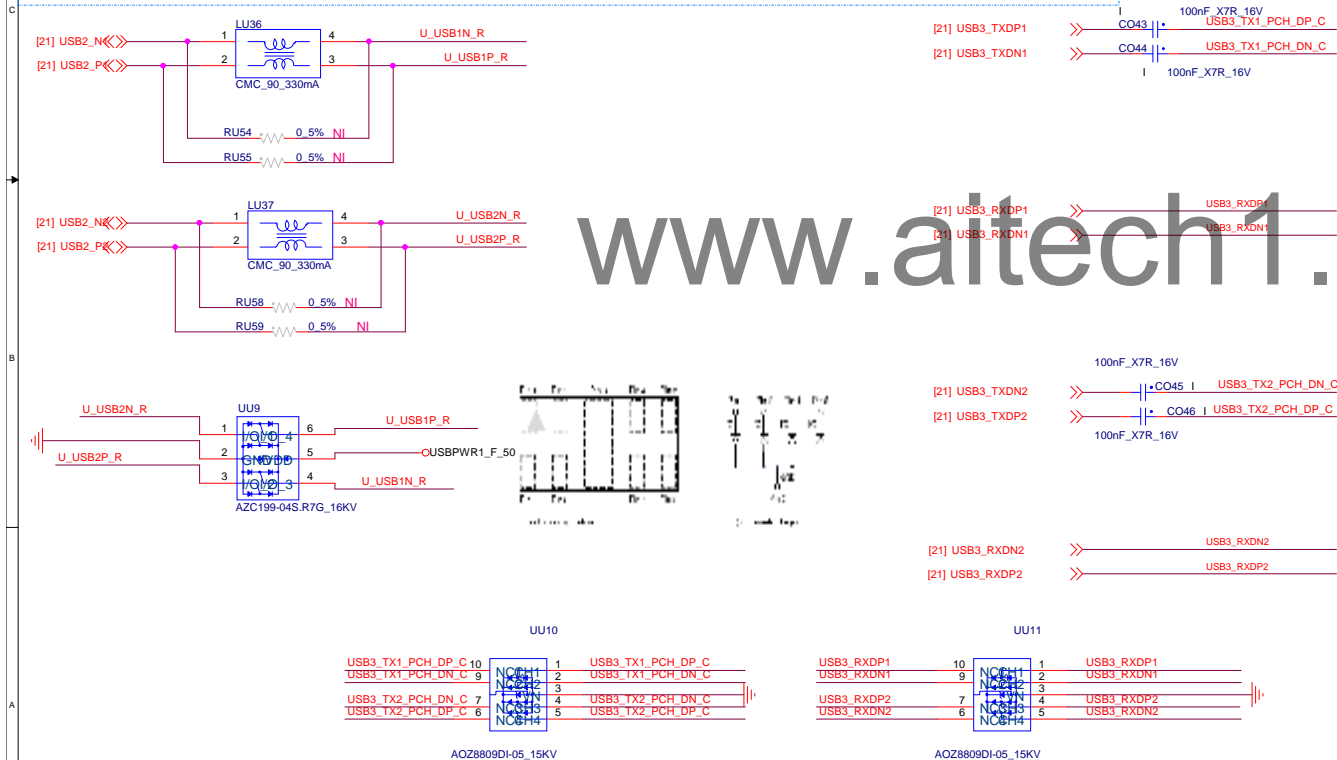
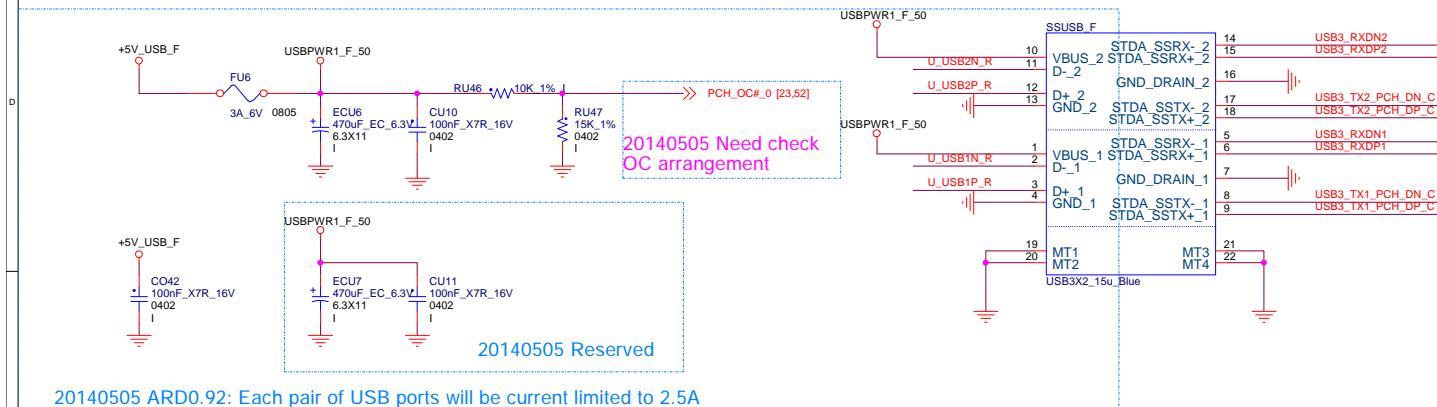
[illegible]

Testing		
ATS Criteria	Test	Interpret
Pr-1	McNemar's	Can we reject H ₀ = no diff
Pr-2	McNemar's	multinomial test (if system is in 3)
Pr-2	McNemar's	used for determining if system is in group 3
Pr-3	McNemar's	used for determining if system is in 3
Pr-4	McNemar's	multinomial test (if system is in 3)
Pr-5	McNemar's	multinomial test (if system is in 3)
Pr-6	McNemar's	Used
Pr-7	McNemar's	Used
Pr-8	McNemar's	Used
Pr-9	McNemar's	Used
Pr-10	McNemar's	Used
Pr-11	McNemar's	Used
Pr-12	McNemar's	Used
Pr-13	McNemar's	Used
Pr-14	McNemar's	Used
Pr-15	McNemar's	Used
Pr-16	McNemar's	Used
Pr-17	McNemar's	Used
Pr-18	McNemar's	Used
Pr-19	McNemar's	Used
Pr-20	McNemar's	Used
Pr-21	McNemar's	Used
Pr-22	McNemar's	Used
Pr-23	McNemar's	Used
Pr-24	McNemar's	Used
Pr-25	McNemar's	Used
Pr-26	McNemar's	Used
Pr-27	McNemar's	Used
Pr-28	McNemar's	Used
Pr-29	McNemar's	Used
Pr-30	McNemar's	Used
Pr-31	McNemar's	Used
Pr-32	McNemar's	Used
Pr-33	McNemar's	Used
Pr-34	McNemar's	Used
Pr-35	McNemar's	Used
Pr-36	McNemar's	Used
Pr-37	McNemar's	Used
Pr-38	McNemar's	Used
Pr-39	McNemar's	Used
Pr-40	McNemar's	Used
Pr-41	McNemar's	Used
Pr-42	McNemar's	Used
Pr-43	McNemar's	Used
Pr-44	McNemar's	Used
Pr-45	McNemar's	Used
Pr-46	McNemar's	Used
Pr-47	McNemar's	Used
Pr-48	McNemar's	Used
Pr-49	McNemar's	Used
Pr-50	McNemar's	Used
Pr-51	McNemar's	Used
Pr-52	McNemar's	Used
Pr-53	McNemar's	Used
Pr-54	McNemar's	Used
Pr-55	McNemar's	Used
Pr-56	McNemar's	Used
Pr-57	McNemar's	Used
Pr-58	McNemar's	Used
Pr-59	McNemar's	Used
Pr-60	McNemar's	Used
Pr-61	McNemar's	Used
Pr-62	McNemar's	Used
Pr-63	McNemar's	Used
Pr-64	McNemar's	Used
Pr-65	McNemar's	Used
Pr-66	McNemar's	Used
Pr-67	McNemar's	Used
Pr-68	McNemar's	Used
Pr-69	McNemar's	Used
Pr-70	McNemar's	Used
Pr-71	McNemar's	Used
Pr-72	McNemar's	Used
Pr-73	McNemar's	Used
Pr-74	McNemar's	Used
Pr-75	McNemar's	Used
Pr-76	McNemar's	Used
Pr-77	McNemar's	Used
Pr-78	McNemar's	Used
Pr-79	McNemar's	Used
Pr-80	McNemar's	Used
Pr-81	McNemar's	Used
Pr-82	McNemar's	Used
Pr-83	McNemar's	Used
Pr-84	McNemar's	Used
Pr-85	McNemar's	Used
Pr-86	McNemar's	Used
Pr-87	McNemar's	Used
Pr-88	McNemar's	Used
Pr-89	McNemar's	Used
Pr-90	McNemar's	Used
Pr-91	McNemar's	Used
Pr-92	McNemar's	Used
Pr-93	McNemar's	Used
Pr-94	McNemar's	Used
Pr-95	McNemar's	Used
Pr-96	McNemar's	Used
Pr-97	McNemar's	Used
Pr-98	McNemar's	Used
Pr-99	McNemar's	Used
Pr-100	McNemar's	Used




Front USB/LED Header


SFF



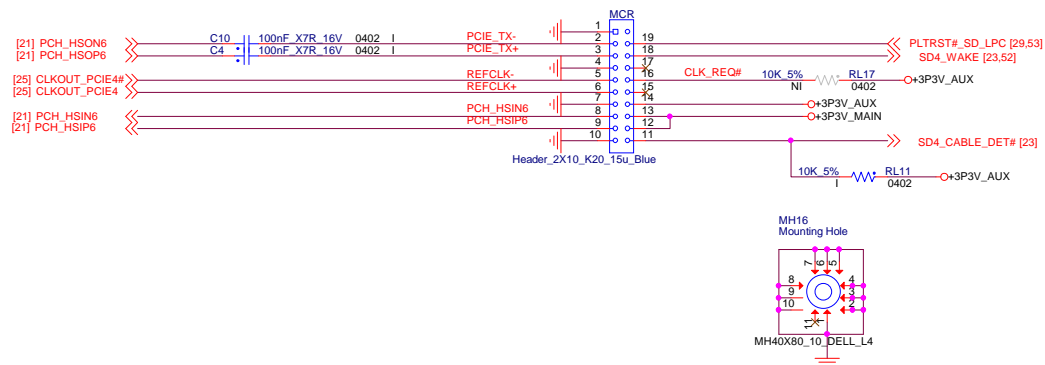
www.aitech1.ru

	
Title	
FRONT_USB3.0	
DWG NO	Rev
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www.aitech1.ru

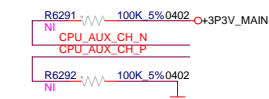
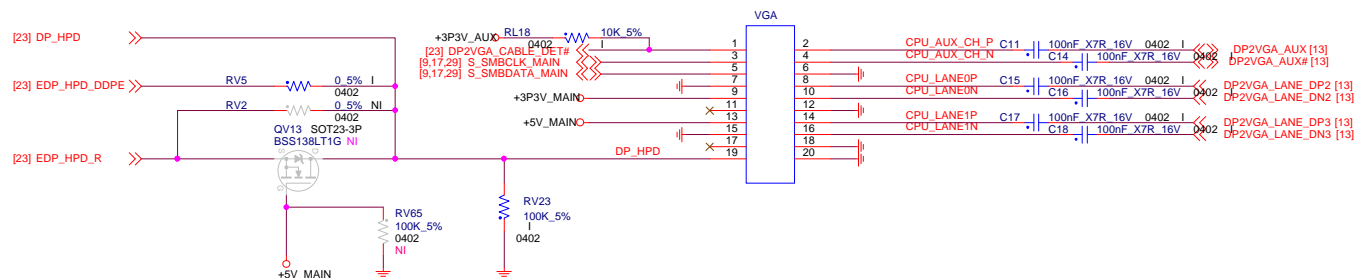
		
Ver	M2	
Doc No	Farallon SFF	A00
Rev	1.0	1.0

SD4.0 CONN



eDP to VGA CONN
M/B part already OK

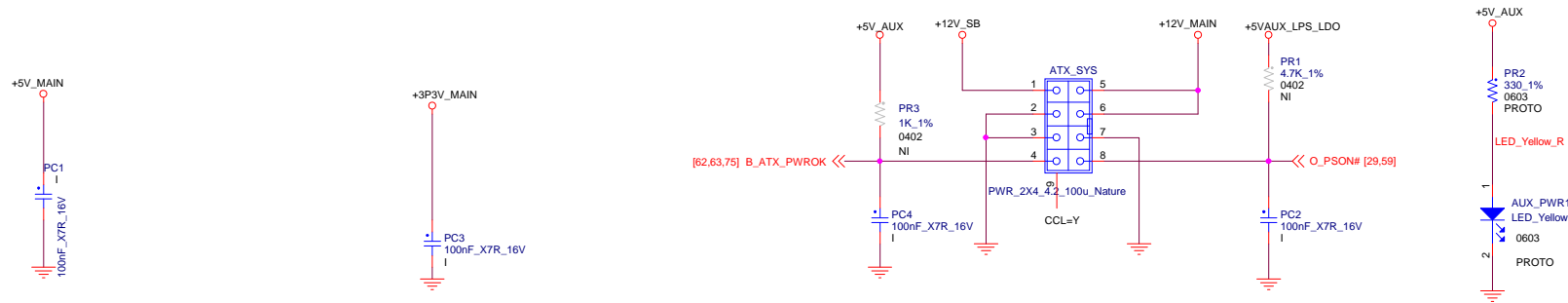
www.aitech1.ru



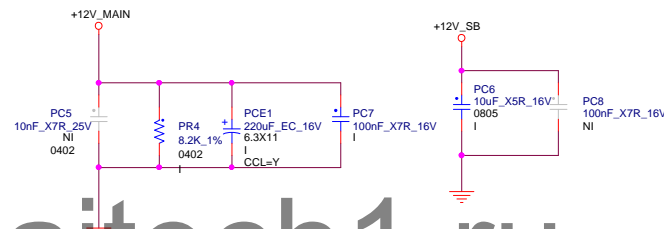
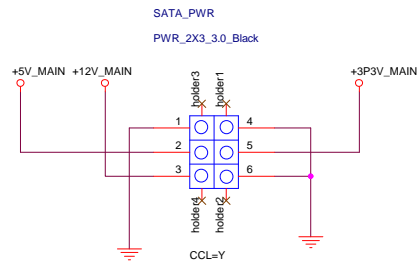
20140515 reserved for AUX

Title	
SD4.0 CON/ DP TO VGA CON	
DWG NO	Rev
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ATX POWER CONNECTOR

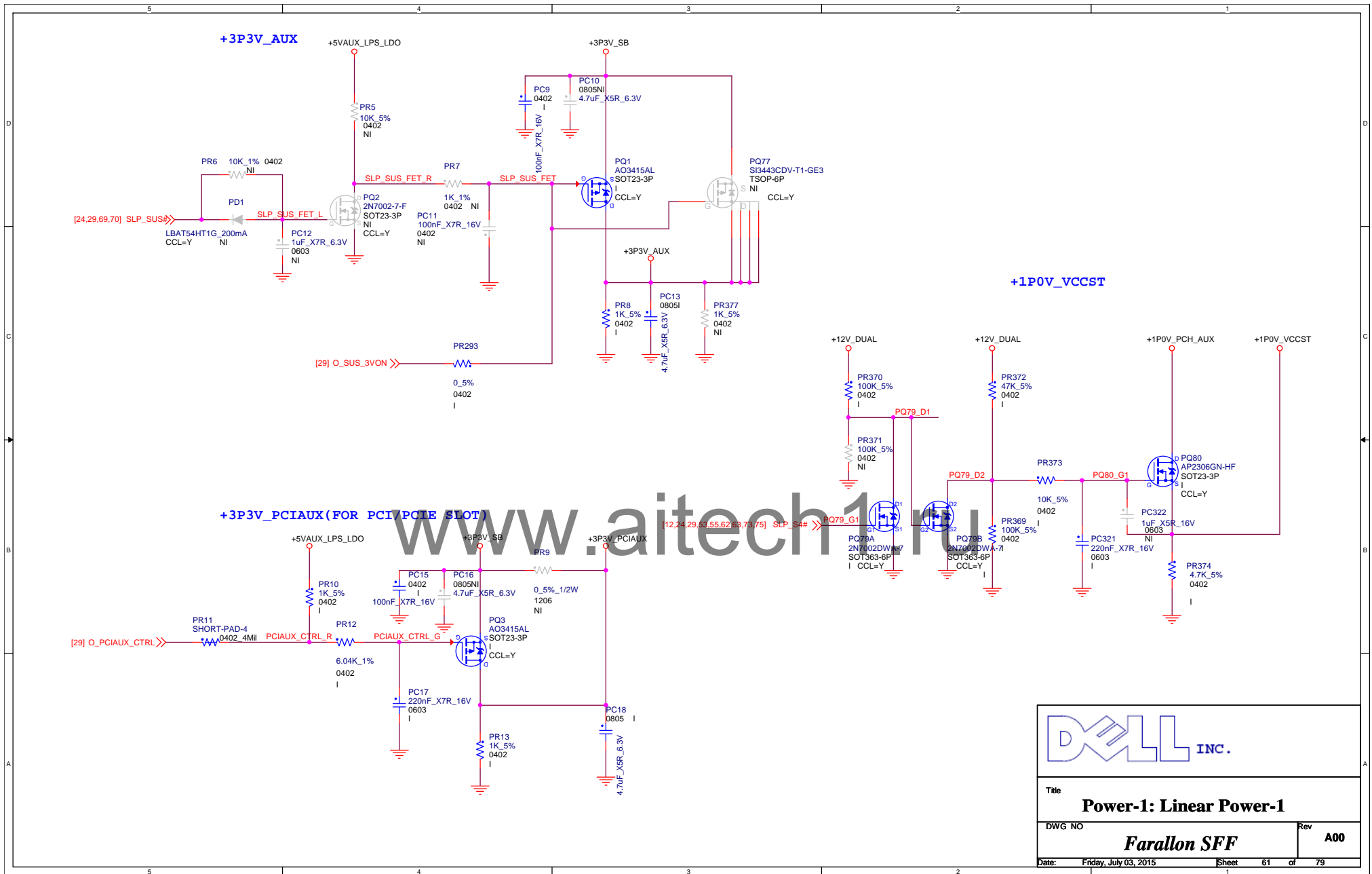


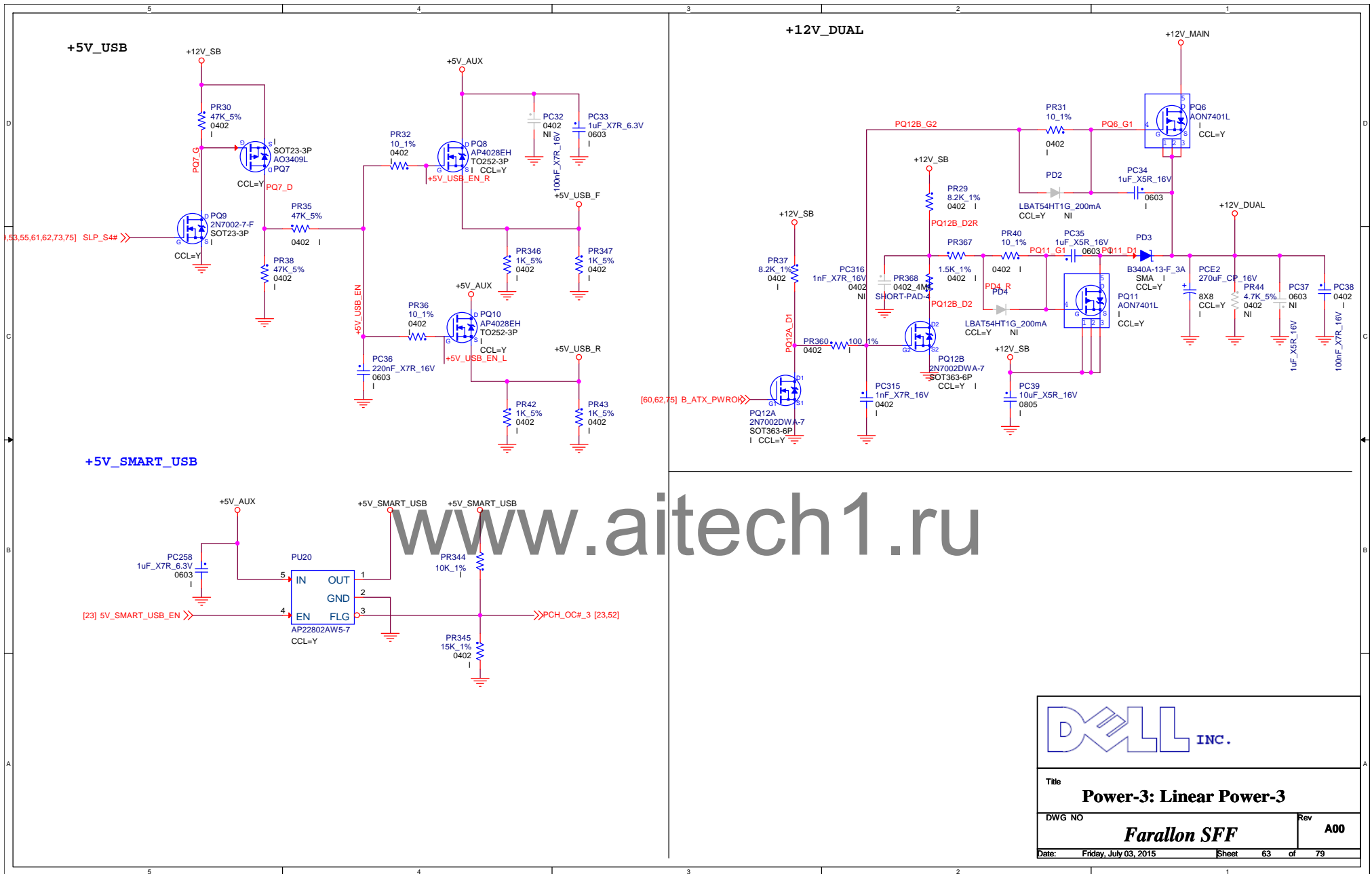
For ODD and HDD For SFF

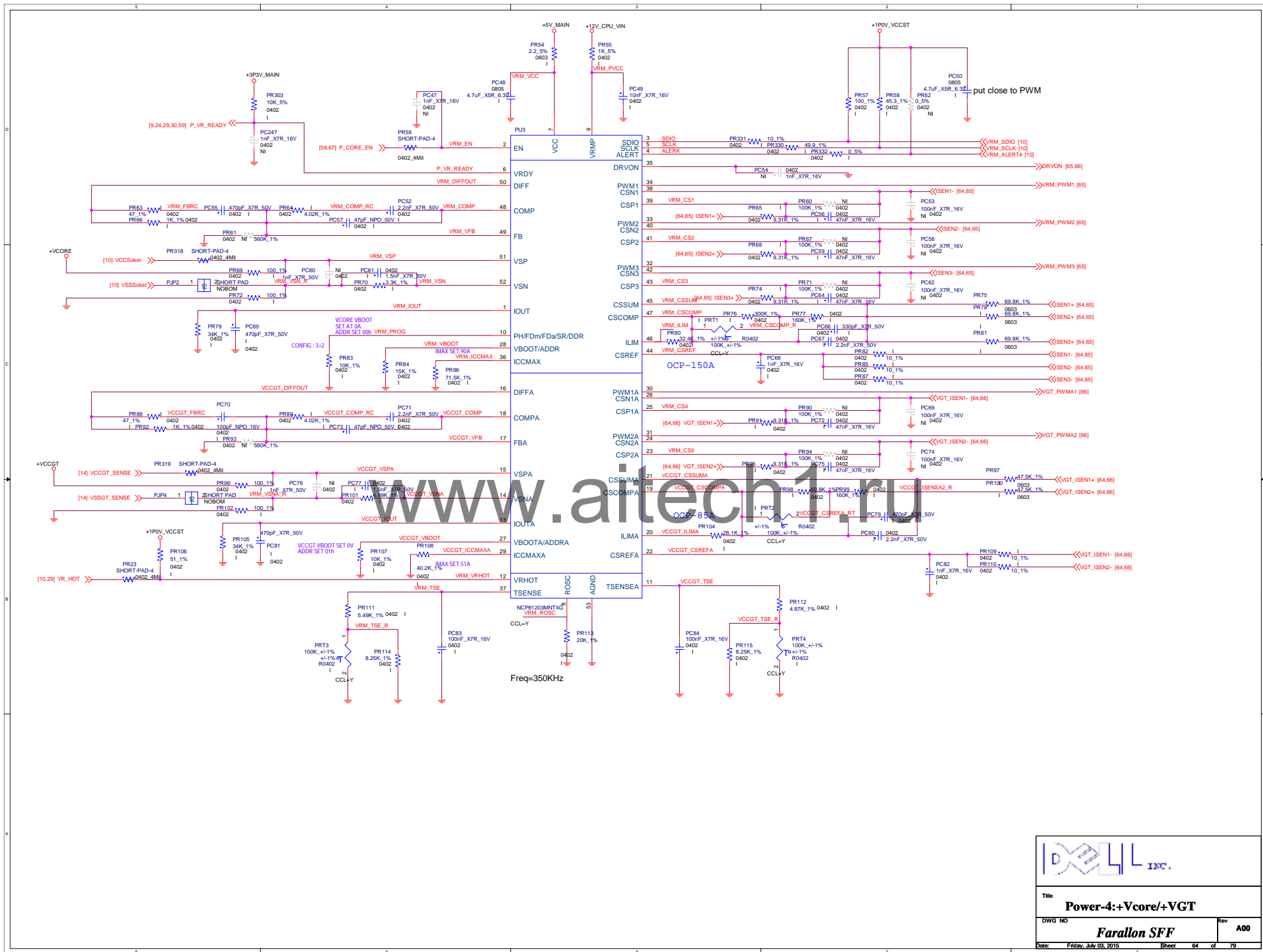


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Title		
Power CONN		
DWG NO	Rev	A00
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Power-4: +Vcore/+VGT

DWG NO: **Farallon SFF**

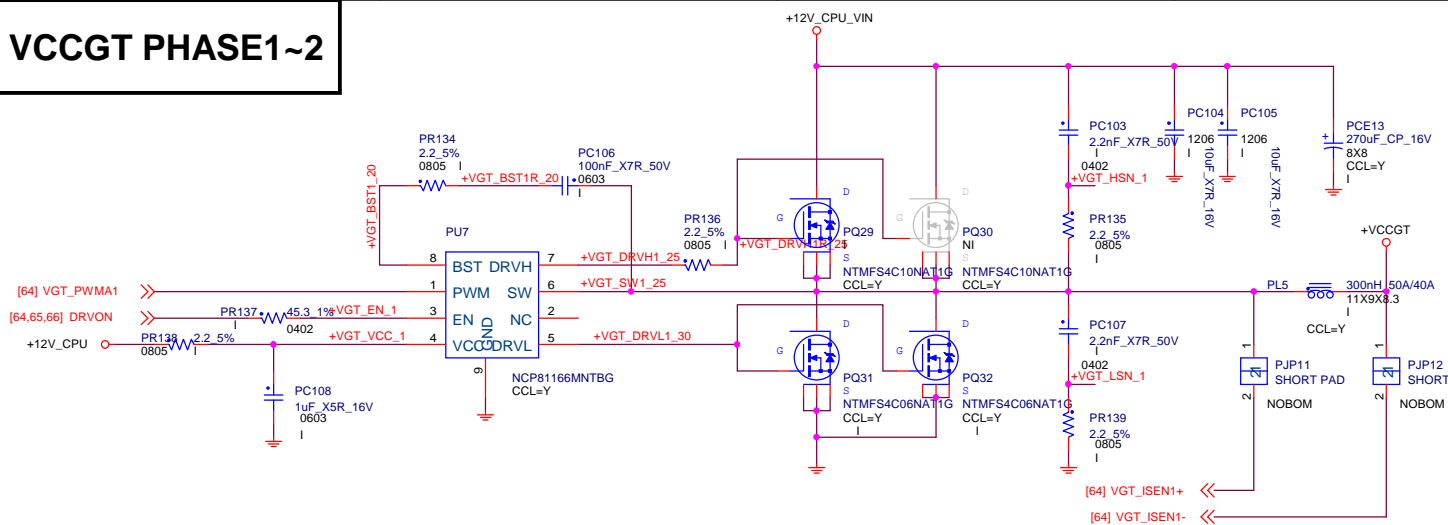
Date: Friday, July 13, 2018 Sheet: 04 of 79

VCORE PHASE1~3

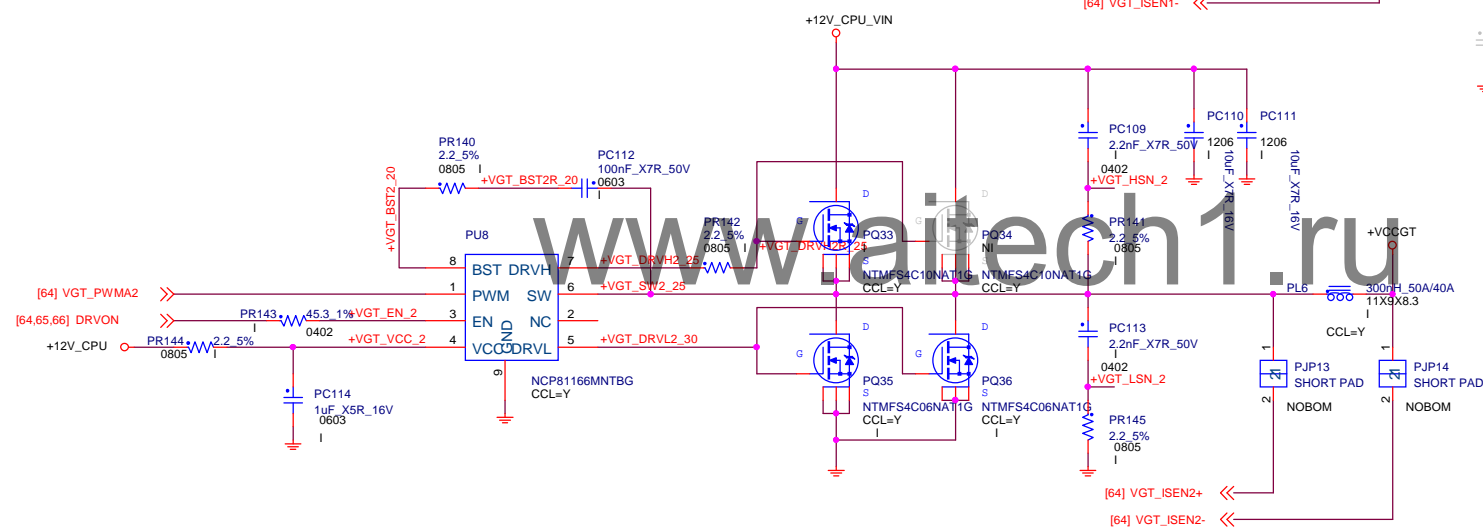
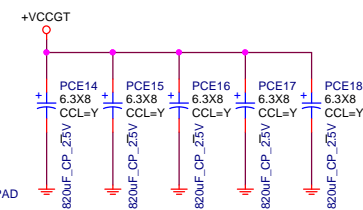


Title		
Power-5:+Vcore Driver		
DWG NO	<i>Farallon SFF</i>	Rev A00
Date: Friday, July 03, 2015	Sheet 65	of 79

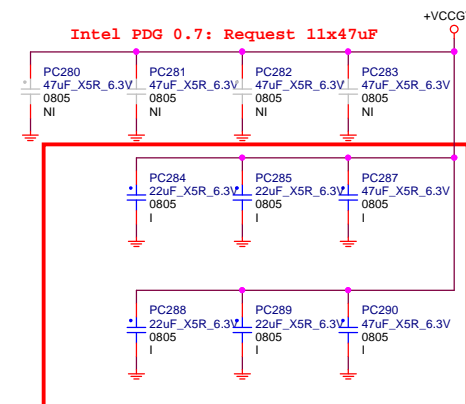
VCCGT PHASE1~2



It_{dc}=34A
I_{max}=51A



Intel PDG 0.7: Request 11x47uF



CPU CAVITY



Title

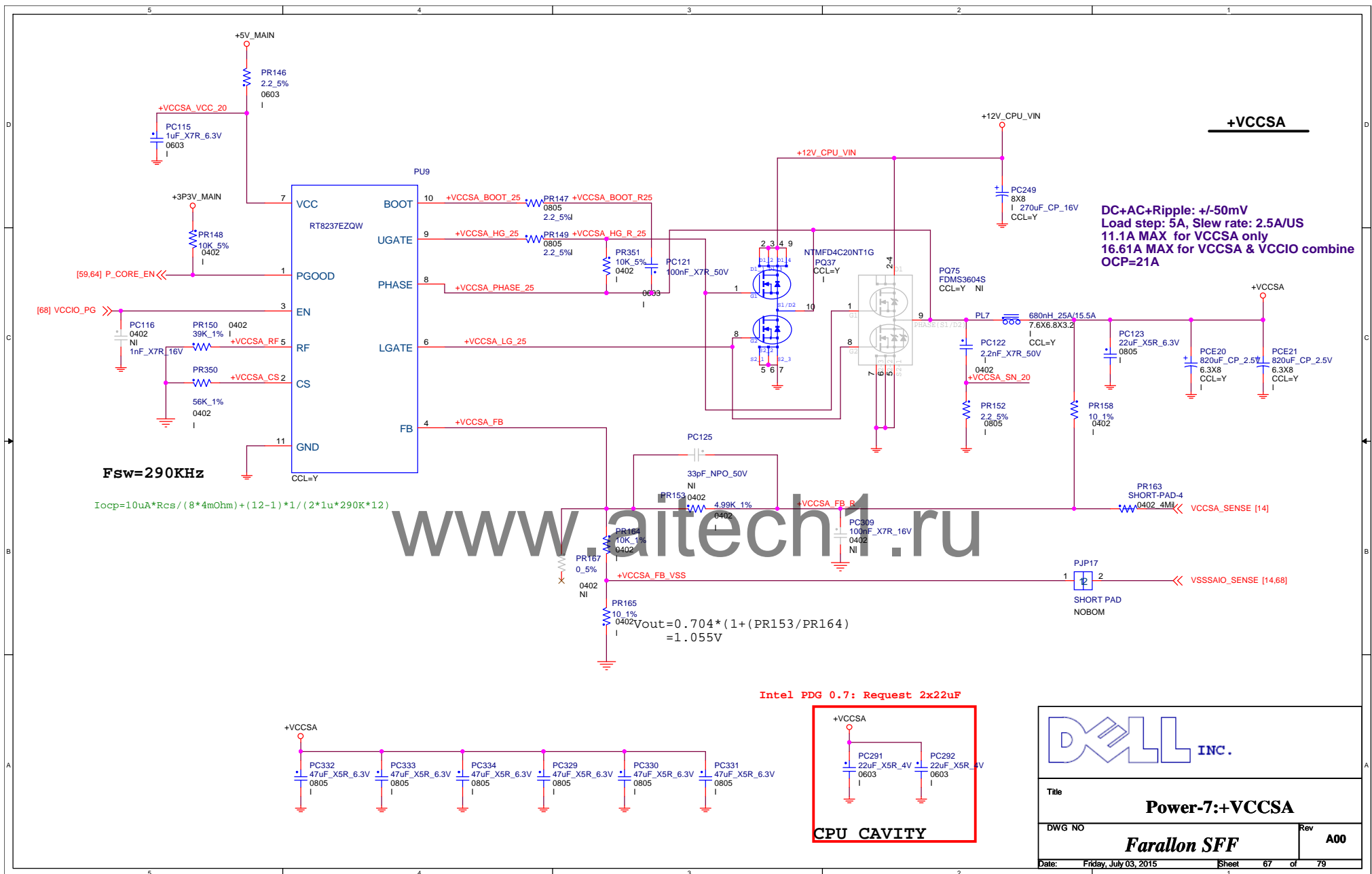
Power-6:+VGT Driver

DWG NO

Farallon SFF

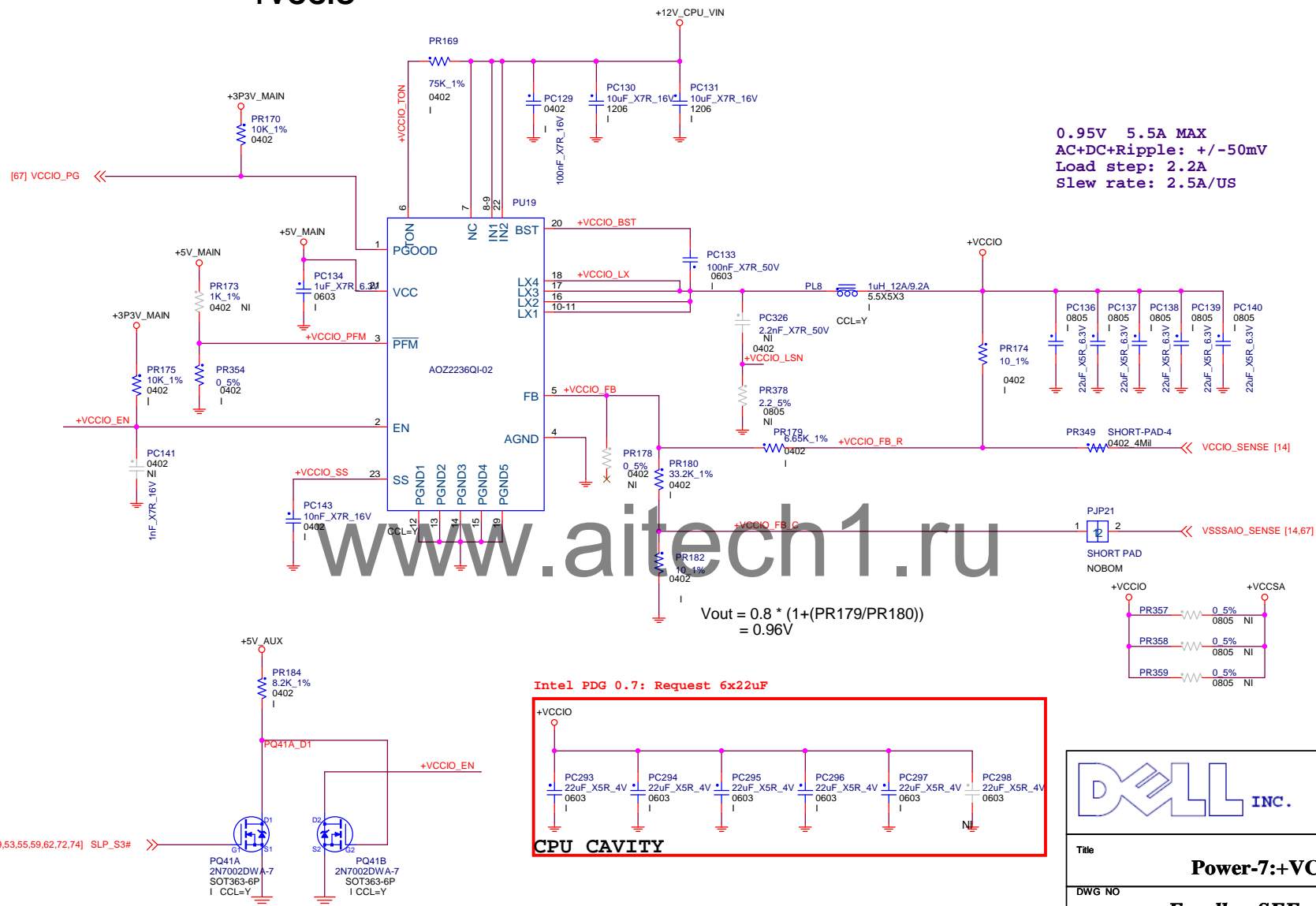
Rev	A00
-----	-----

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+VCCIO

$F_{sw}(KHz) = 38000 \cdot V_{out} / R_{ton}(Kohm) = 450KHz$

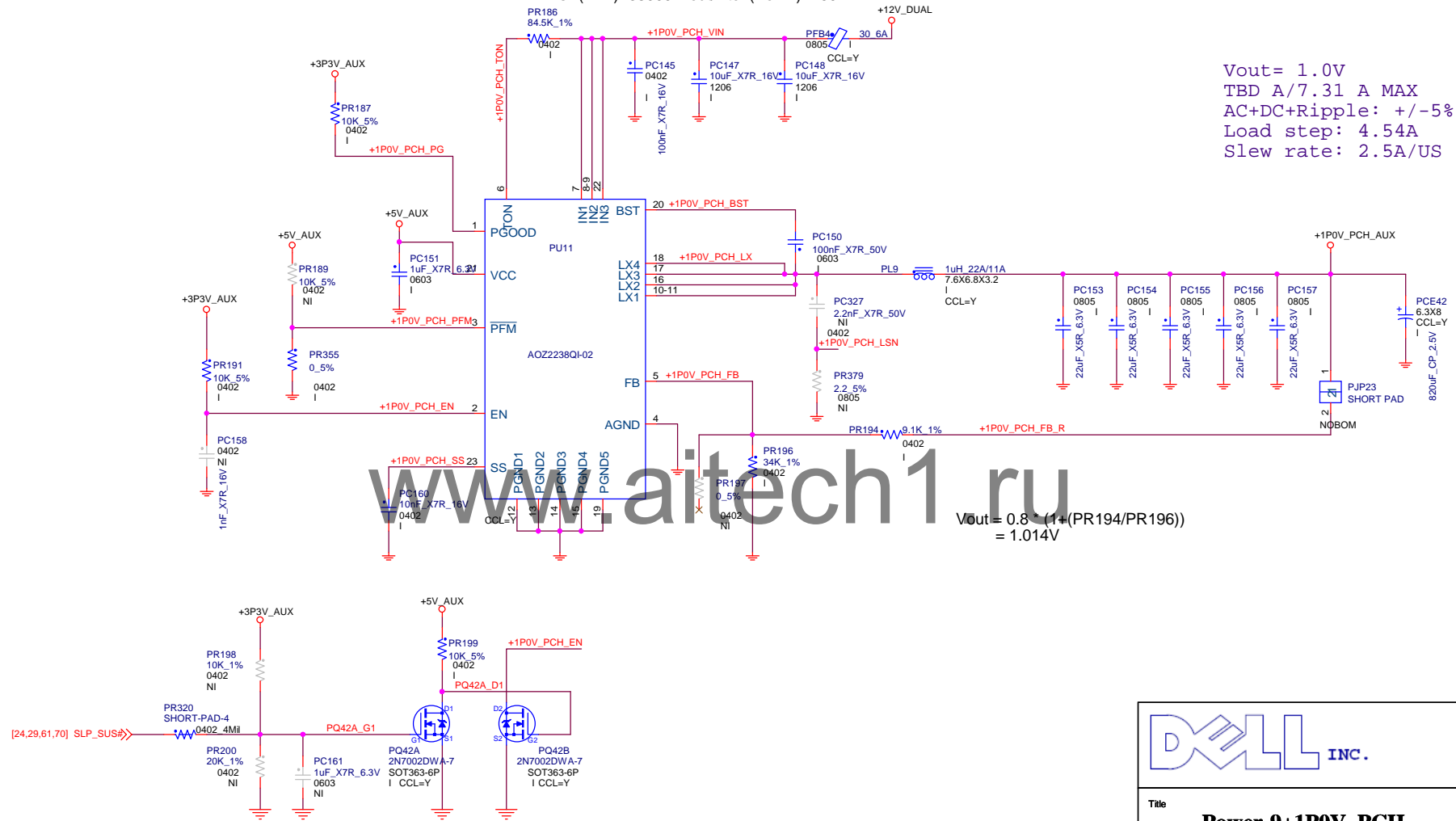


Title		Power-7:+VCCSA	
DWG NO		Farallon SFF	Rev A00
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+1P0V_PCH_AUX

$$F_{sw}(KHz) = 38000 \cdot V_{out} / R_{ton}(Kohm) = 450KHz$$

Vout = 1.0V
 TBD A/7.31 A MAX
 AC+DC+Ripple: +/-5%
 Load step: 4.54A
 Slew rate: 2.5A/US



$$V_{out} = 0.8 \cdot (1 + (PR194/PR196)) = 1.014V$$

Title		
Power-9+1P0V_PCH		
DWG NO		Rev
Farallon SFF		A00
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5

4

3

2

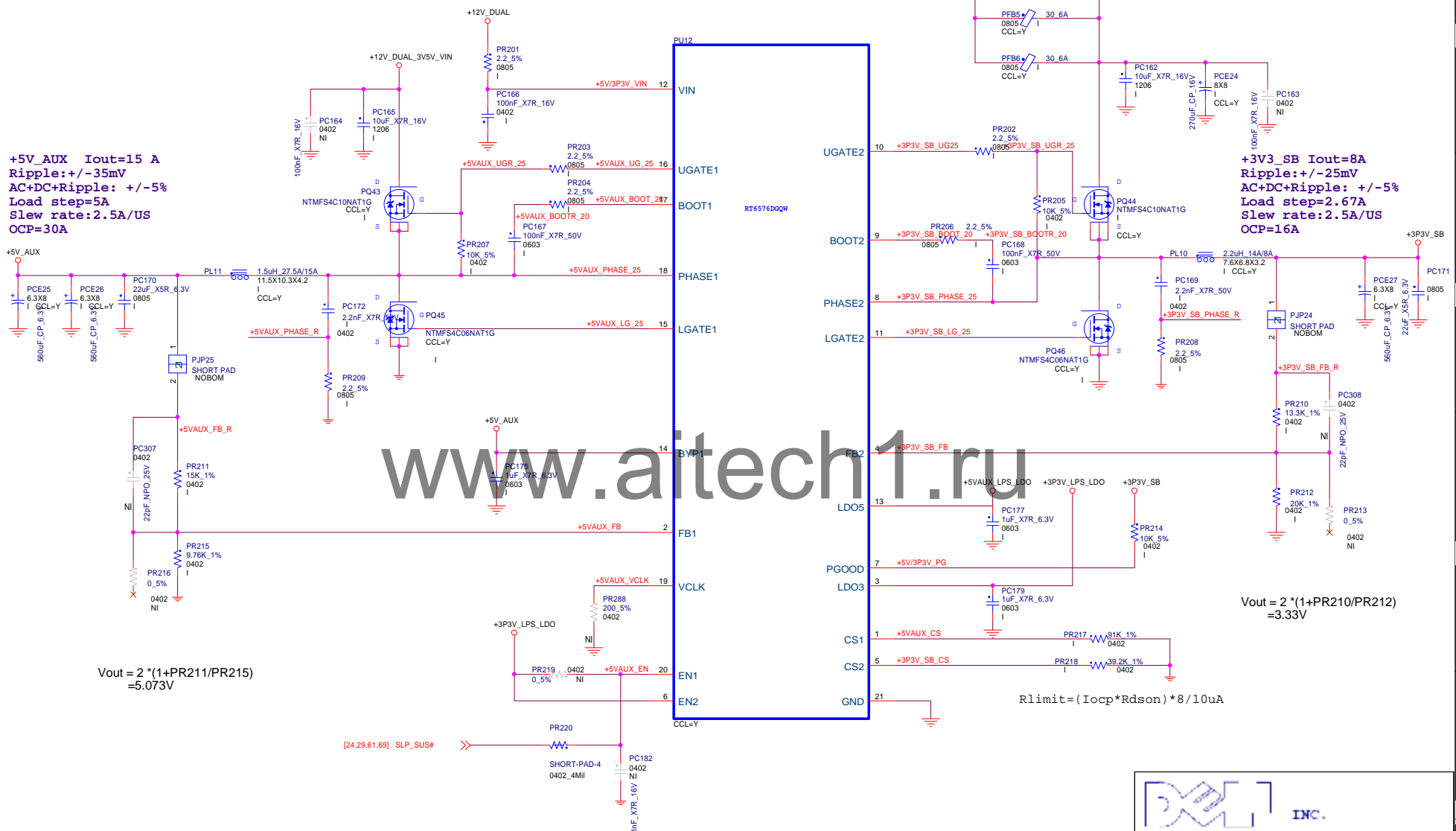
1


D

C

B

A



		
Title		
Power-10:+3P3V_SB/+5V_AUX		
DWG NO	Rev	
	Farallon SFF A00	
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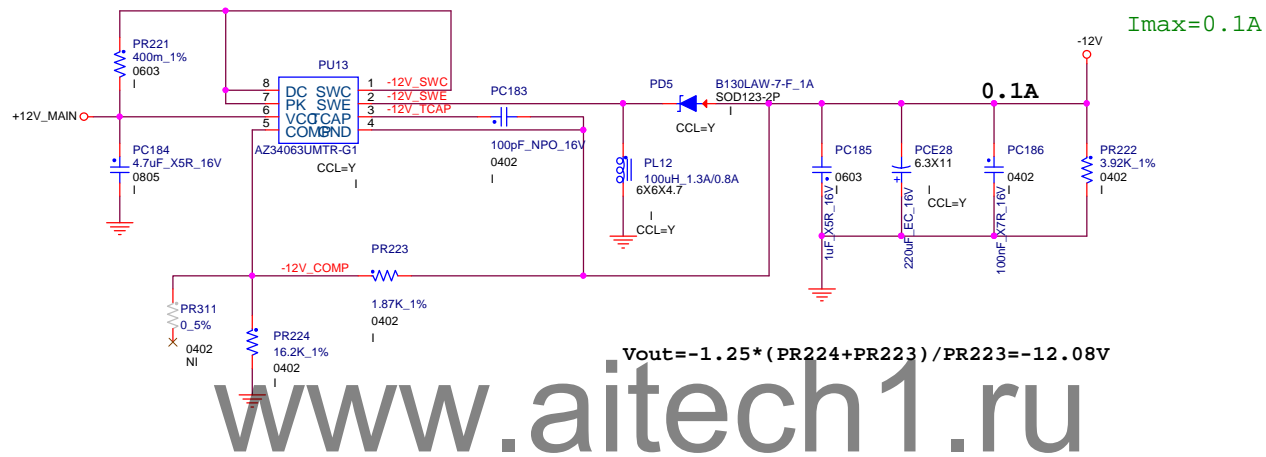
5

4

3

2

1

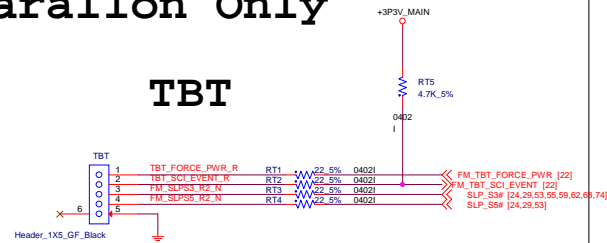


Title		Power-11:-12V	
DWG NO		Rev A00	
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PCB1
Printed Circuit Board
PCB_D6 KINGCOBRA
CCL=Y

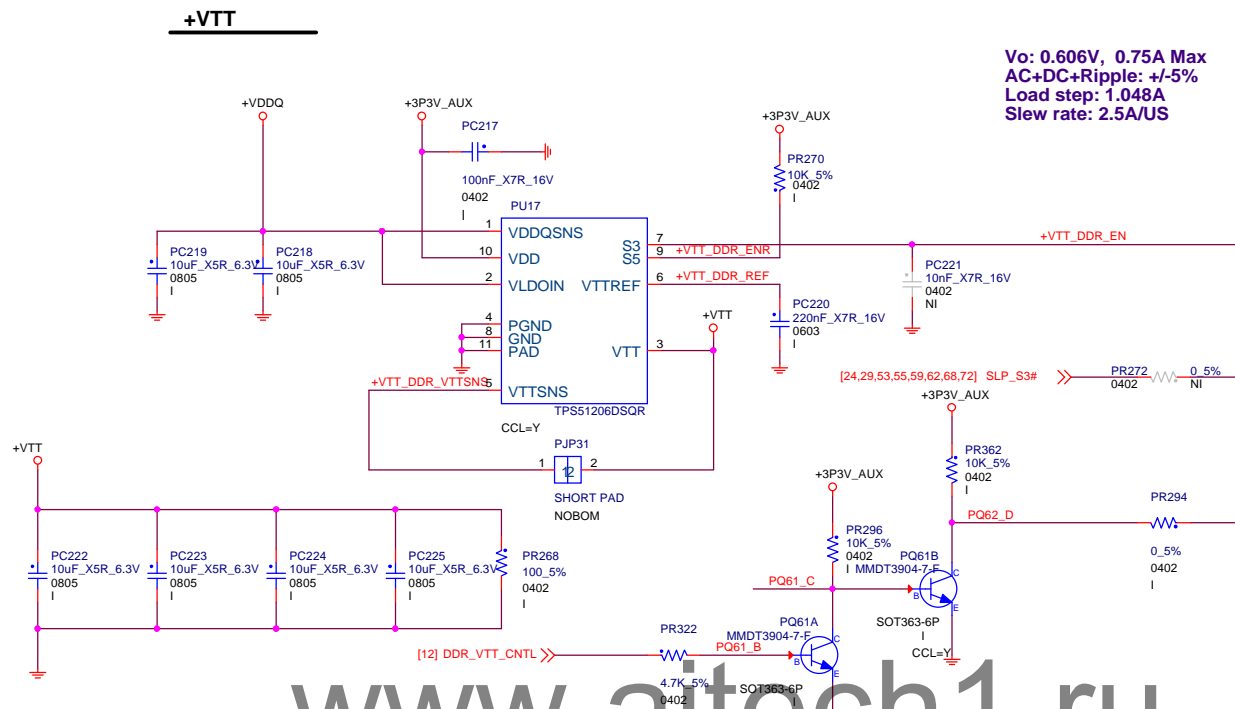
Farallon Only

TBT




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Title TBT	
DWG NO Farallon SFF	Rev A00
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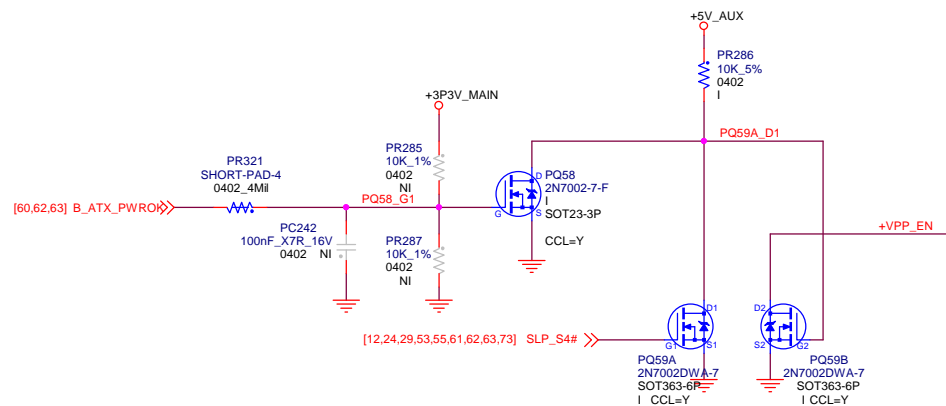
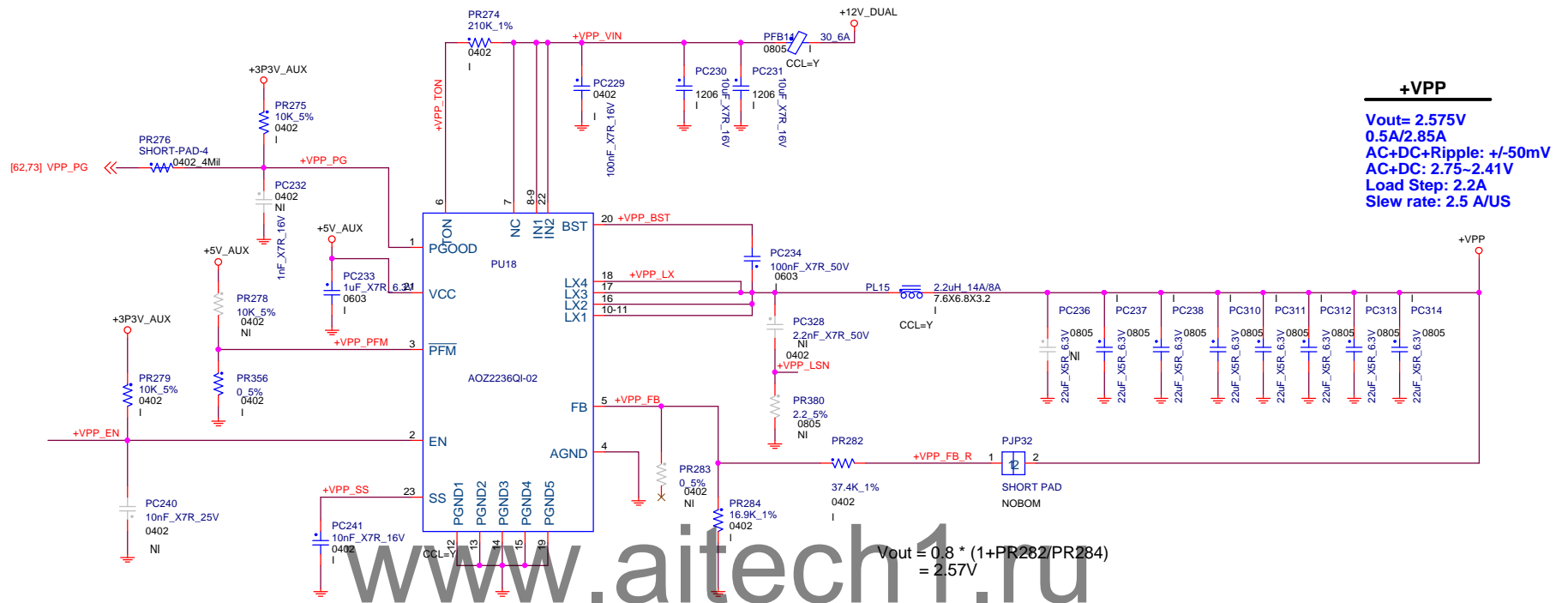


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Power-15:DDR4 +VTT_DDR		
DWG NO	Farallon SFF	Rev A00
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+VPP

$$F_{sw}(KHz)=38000 \cdot V_{out}/R_{ton}(Kohm)=450KHz$$



Title		
Power-16:DDR4 +VPP		
DWG NO	Rev	A00
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